SERVICE MANUAL

7941 AND 7945 DISC DRIVES

Manual part no. 07940-90903
Microfiche part no. 07940-90803

PRINTED: SEP 1985 07940-90903
Printed in U.S.A E0985

HEWLETT PACKARD

PRINTING HISTORY

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Serial Number Prefix

The main part of this manual applies directly to HP 7941 and HP 7945 Disc Drives with serial numbers prefixed 2540 and subsequent. Refer to Appendix B for disc drives with serial numbers prefixed 2515 and prior. Refer to Appendix A for disc drives with serial numbers prefixed 2438 and prior.

OPTIONS COVERED

In addition to the standard models, this manual covers the following options: 015 and 550.

FOR U.S.A. ONLY

The Federal Communications Commission (in 47 CFR 15.838) has specified that the following notice be brought to the attention of the users of this product.

FEDERAL COMMUNICATIONS COMMISSION
RADIO FREQUENCY INTERFERENCE
STATEMENT

Warning: This equipment generates and uses radio frequency energy and if not installed and used properly, that is, in strict accordance with the manufacturer's instructions, may cause interference to radio and television reception. It has been type tested and found to comply with the limits for a Class B computing device in accordance with the specifications in Subpart J of Part 15 of FCC Rules, which are designed to provide reasonable protection against such interference in a residential installation. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures: reorient the receiving antenna; relocate the computer with respect to the receiver; move the computer away from the receiver; plug the computer into a different branch circuit. If necessary, the user should consult the dealer or authorized field service representative for additional suggestions. The user may find the following booklet prepared by the Federal Communications Commission helpful: "How to Identify and Resolve Radio-TV Interference Problems". This booklet is available from the U.S. Government Printing Office, Washington, DC 20402. Stock No. 004-000-00345-4.

HEWLETT-PACKARD COMPANY
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SAFETY CONSIDERATIONS

GENERAL - This product and related documentation must be reviewed for familiarization with safety markings and instructions before operation.

SAFETY SYMBOLS

Instruction manual symbol: the product will be marked with this symbol when it is necessary for the user to refer to the instruction manual in order to protect the product against damage.

Indicates hazardous voltages.

Indicates earth (ground) terminal.

WARNING The WARNING sign denotes a hazard. It calls attention to a procedure or practice which, if not correctly performed or adhered to, could result in personal injury. Do not proceed beyond a WARNING sign until the indicated conditions are fully understood and met.

CAUTION The CAUTION sign denotes a hazard. It calls attention to an operating procedure or practice which, if not correctly performed or adhered to, could result in damage to or destruction of part or all of the product. Do not proceed beyond a CAUTION sign until the indicated conditions are fully understood and met.

SAFETY EARTH GROUND - This is a safety class I product and is provided with a protective earthing terminal. An uninterruptible safety earth ground must be provided from the main power source to the product input wiring terminals, power cord, or supplied power cord set. Whenever it is likely that the protection has been impaired, the product must be made inoperative and be secured against any unintended operation.

BEFORE APPLYING POWER - Verify that the product is configured to match the available main power source according to the input power configuration instructions provided in this manual.

If this product is to be operated with an autotransformer make sure that the common terminal is connected to the earth terminal of the main power source.

SERVICING

WARNING

Any servicing, adjustment, maintenance, or repair of this product must be performed only by service-trained personnel.

Adjustments described in this manual may be performed with power supplied to the product while protective covers are removed. Energy available at many points may, if contacted, result in personal injury.

Capacitors inside this product may still be charged after the product has been disconnected from the main power source.

To avoid a fire hazard, fuses with the proper current rating and of the specified type (normal blow, time delay, etc.) must be used for replacement.

To install or remove a fuse, first disconnect the power cord from the device. Then, using a small flat-bladed screw driver, turn the fuseholder cap counterclockwise until the cap releases. Install either end of a properly rated fuse into the cap. Next, insert the fuse and fuseholder cap into the fuseholder by pressing the cap inward and then turning it clockwise until it locks in place.

GENERAL INFORMATION

SECTION I

1-1. INTRODUCTION

The Hewlett-Packard 7941 and 7945 Disc Drives are medium performance, random access, data storage devices designed for use with small and medium sized computer systems. The formatted storage capacities of the HP 7941 and HP 7945 are 24 megabytes and 55 megabytes, respectively. In this manual, unless otherwise specified, "disc drive" refers to both the HP 7941 and HP 7945.

The disc drive employs two (HP 7941) or four (HP 7945) nonremovable 130-millimetre (5.12-inch) discs for storage media. Each disc surface employs one movable head to service its data tracks. The bottom surface of the lowest disc in the stack contains continuous prerecorded servo data which is used to ensure the precise positioning of the read/write heads.

Head positioning is performed by a rotary actuator and a closed-loop servo positioning system. Mechanical and contamination protection for the discs, heads, and the rotary actuator is provided by a sealed head-disc module. The head-disc module includes a self-contained air filtration system which supplies clean air and temperature equalization throughout the module.

Also included in the disc drive are a Hewlett-Packard Interface Bus (HP-IB)* controller and a power supply.

The disc drive contains internal self-test diagnostics and a fault-finding system which exercise key functions of the disc drive. Self test is performed automatically at power on and can also be initiated by the host or by a switch on the rear panel of the unit. Go/no-go test results are indicated by a green/red indicator on the front panel. If a failure occurs, information on the cause of the failure can be determined by viewing a 2-digit hexadecimal display on the rear panel.

The disc drive is packaged in a stand-alone desktop cabinet. Accessories available include a desk-height stand-alone cabinet designed to hold the disc drive and other desktop stack modules. A kit for rack mounting the disc drive in a standard EIA equipment rack is also available.

This manual provides all the service information needed to maintain the disc drive. Details of the control functions provided by the host computer are described in the installation documentation provided with the computer.

1-2. SCOPE OF MANUAL

The manual is divided into six sections as follows:

a. Section I contains a general description of the disc drive.

b. Section II provides information about the CS/80 Instruction Set and the Hewlett-Packard Interface Bus (HP-IB).

c. Section III describes the operating principles of the disc drive.

d. Section IV contains servicing information for the disc drive, including instructions on how to use the internal diagnostics.

e. Section V supplies step-by-step removal and replacement procedures for all field-replaceable assemblies and parts in the disc drive.

f. Section VI lists and illustrates all of the field-replaceable assemblies and parts in the disc drive.

Appendix A contains backdating information about removal and replacement and replaceable parts for HP 7941 and HP 7945 Disc Drives with serial numbers prefixed with 2438 and prior.

Appendix B contains backdating information about theory of operation, service information, removal and replacement, and replaceable parts

*NOTE: Not just IEEE-488, but the hardware, documentation and support that delivers the shortest path to a computation system.

information for HP 7941 and HP 7945 Disc Drives with serial numbers prefixed 2515 and prior.

Appendix C provides a listing and copy of all the service notes applicable to the HP 7941 and HP 7945 Disc Drives.

1-3. OPTIONS

Option 015 is the power option. The only requirement is for the switch in the power module to be placed in the proper position. Option 550 is the deletion of the Model 10833B HP-IB Cable from the order.

1-4. RELATED MANUALS

For operating and installation instructions, refer to the *7941 and 7945 Disc Drive Owner's Manual,* part no. 07940-90901, and the *Site Environmental Requirements for Disc/Tape Drives Manual,* part no. 5955-3456. For instruction set information, refer to the *CS/80 Instruction Set Programming Manual,* part no. 5955-3442. For additional service information, refer to the *CS/80 External Exerciser Reference Manual,* part no. 5955-3462. The CE Handbook for the HP 7941 and HP 7945 Disc Drive is part no. 07940-90905.

1-5. CHARACTERISTICS

Characteristics of the disc drive, including physical dimensions and power requirements, are listed in table 1-1, Disc Drive Characteristics. Detailed specifications for the disc drive, including environmental requirements, are listed in *Site Environmental Requirements for Disc/Tape Drives Manual* , part no. 5955-3456. This publication is supplied with the disc drive.

Table 1-1. Disc Drive Characteristics

SAFETY

Meets all applicable safety standards of IEC 380 and IEC 435.

UL recognized to UL 478.

CSA certified to CSA C22.2 No. 143 and No. 154.

POWER REQUIREMENTS

Specified Source (selected by rear panel VOLTAGE SELECTOR switch)

Voltage (true RMS): 115V range; 100V, 115V, 120V, single phase, (inclusive tolerance range is 90V to 132V)

230V range; 220V, 240V, single phase, (inclusive tolerance range is 180V to 264V)

Frequency: 47.5 to 66 Hz

Typical Current (true RMS): 115V range; 0.87A
230V range; 0.48A

Typical Power: 115V range; 65W
230V range; 65W

SIZE/WEIGHT

Height: 130 mm (5.1 in.)

Width: 325 mm (12.8 in.)

Depth: 285 mm (11.2 in.)

Net Weight: 9.9 kg (21.8 lb)

Shipping Weight: 12.9 kg (28.5 lb)

2-1. INTRODUCTION

Interface to the disc drive is accomplished through Hewlett-Packard Interface Bus (HP-IB) hardware and the CS/80 Instruction Set, a set of commands formulated for mass storage devices. The following paragraphs discuss the types of CS/80 commands. Also provided is an overview of HP-IB. For full details of CS/80, refer to the *CS/80 Instruction Set Programming Manual*, part no. 5955-3442.

2-2. CS/80 INSTRUCTION SET

The increase in capabilities of both host computers and mass storage devices has emphasized the need for efficient channel communication. The CS/80 Instruction Set increases the efficiency and speed of channel operations between disc memories and their associated host computers. Table 2-1, Device Command Summary, provides a summary of all CS/80 instructions. The CS/80 Instruction Set allows a host computer to access special utilities within the disc drive. Utilities are routines stored in firmware which allow error rate tests to be performed and the results of such tests to be examined or logged. Utilities are listed in table 2-2, Disc Drive Utilities. Refer to the *External Exerciser Reference Manual*, part no. 5955-3462, for full details.

2-3. TRANSACTION STRUCTURE

A transaction is a logically complete operation between a system host computer and a peripheral device (the disc drive) over a given channel (HP-IB). Three phases may occur during each transaction: command, execute, and report. A transaction begins when a command is received by the disc drive, and ends when a reporting message indicating the status of the transaction is accepted by the host. Figure 2-1 illustrates the transaction structure, and shows the relationship between the disc drive operating states and the channel activity relative to each phase.

A unit is a separately addressable entity within a device (disc drive). A volume is a separately addressable portion of the storage media within a given unit.

2-4. REAL TIME COMMANDS

Real time commands are optimized for execution time. These commands are used most often in host/device transactions. One or more complementary commands may precede a real time command in order to modify the operation of that command. Real time commands include: locate and read, locate and write, and cold load read.

2-5. COMPLEMENTARY COMMANDS

Complementary commands are used to set or update programmable states in the disc drive. The programmable states define characteristics such as: set unit, set address, set block displacement, set return addressing mode, set length, set burst mode, set retry time, set release, set status mask, and set Rotational Position Sensing (RPS) window size. These commands may be included within Real Time, General Purpose, or Diagnostic command messages, or they may stand alone.

When a complementary command (or commands) is embedded within another command, the parameters or conditions established by that complementary command(s) are altered only for the duration of the current command. A stand-alone complementary command, however, sets the parameters or conditions until the same stand-alone complementary command alters the set value or until power-on occurs. Power-on resets all complementary commands to their default values. Therefore, at power-on, length is defaulted to equal the entire volume. A stand-alone Set Length command may give it a "set" value of 1 kbyte to be used for an entire sequence of transactions, although some special case commands could temporarily override this value with an embedded complementary command to set a "current" value of 256 bytes (for 1 sector).

Table 2-1. Device Command Summary

LOCATE AND READ (REAL TIME)

FUNCTION: Locates the data indicated by the target address and transmits the data to the host.

OPCODE: 0_{10} 00000000_2 000_8 00_{16}

FORMAT: No variables or parameters

LOCATE AND WRITE (REAL TIME)

FUNCTION: Tranfers data from the host for storage beginning at the address specified by the target address.

OPCODE: 2_{10} 00000010_2 002_8 02_{16}

FORMAT: No variables or parameters

LOCATE AND VERIFY (GENERAL PURPOSE)

FUNCTION: Instructs the device to perform an internal verification of a section of data to ensure that it can be read.

OPCODE: 4_{10} 00000100_2 004_8 04_{16}

FORMAT: No variables or parameters

SPARE BLOCK (GENERAL PURPOSE)

FUNCTION: Gives the device permission to become temporarily busy while sparing the block indicated by the target address.

OPCODE: 6_{10} 00000110_2 006_8 06_{16}

FORMAT: <00000110> $\langle 00000S0T\rangle_{P1}$

P1 = sparing mode byte
S = 0 skip spare S = 1 jump spare
T = 0 retain data T = 1 do not retain data
T must equal 1 for tape operation
S must equal 0 for disc operation

Table 2-1. Device Command Summary (continued)

COLD LOAD READ (REAL TIME)

FUNCTION: Used by the host to bootstrap itself into a higher operating environment from a more primitive state.

OPCODE: 10_{10} 00001010_2 012_8 $0A_{16}$

FORMAT: No variables or parameters

REQUEST STATUS (DIAGNOSTIC)

FUNCTION: Instructs the device to return (in an execution message) the status report.

OPCODE: 13_{10} 00001101_2 015_8 $0D_{16}$

FORMAT: No variables or parameters

RELEASE (GENERAL PURPOSE)

FUNCTION: Releases the device.

OPCODE: 14_{10} 00001110_2 016_8 $0E_{16}$

FORMAT: No variables or parameters

RELEASE DENIED (GENERAL PURPOSE)

FUNCTION: Prohibits the device from releasing itself.

OPCODE: 15_{10} 00001111_2 017_8 $0F_{16}$

FORMAT: No variables or parameters

Table 2-1. Device Command Summary (continued)

SET ADDRESS (COMPLEMENTARY)

FUNCTION: Used to set the value of the target address and to define the addressing mode.

OPCODE:

16_{10}	00010000_2	020_8	10_{16}
17_{10}	00010001_2	021_8	11_{16}

FORMAT: <0001000T> < P1 > - - - - < P6 >

T = address mode (0 = single vector; 1 = 3-vector)
Single vector format: 6-byte binary number
3-vector format: P1-P3 = cylinder address
P4 = head address
P5-P6 = sector address

SET BLOCK DISPLACEMENT (COMPLEMENTARY)

FUNCTION: Adjusts the target address by the number of blocks indicated by the parameter field.

OPCODE: 18_{10} 00010010_2 022_8 12_{16}

FORMAT: <00010010> < P1 > - - - - < P6 >

Parameter format: 6-byte, signed, two's complement, binary number

SET LENGTH (COMPLEMENTARY)

FUNCTION: Defines the number of bytes in a data transfer.

OPCODE: 24_{10} 00011000_2 030_8 18_{16}

FORMAT: <00011000> < P1 > - - - - < P4 >

Parameter format: 4-byte, unsigned, binary number

Table 2-1. Device Command Summary (continued)

SET UNIT (COMPLEMENTARY)

FUNCTION: Used to specify a specific unit within the device.

OPCODE:

32_{10}	00100000_2	040_8	20_{16}
33_{10}	00100001_2	041_8	21_{16}
47_{10}	00101111_2	057_8	$2F_{16}$

FORMAT: <0010YYYY>

YYYY = unit number (1111 = device controller)

INITIATE UTILITY (DIAGNOSTIC)

FUNCTION: Directs the device to perform one utility routine.

OPCODE:

48_{10}	00110000_2	060_8	30_{16}
49_{10}	00110001_2	061_8	31_{16}
50_{10}	00110010_2	062_8	32_{16}

FORMAT: <001000XX> < P1 > < n parameter bytes >

XX = execution message qualifier
- 00 = no execution message
- 01 = device will receive execution message
- 10 = device will send execution message

P1 = utility number (device specific)
There can be up to 8 bytes in the parameter field. The number and content of these bytes is determined by P1.

INITIATE DIAGNOSTIC (DIAGNOSTIC)

FUNCTION: Directs the device to perform one internally defined diagnostic routine.

OPCODE: 51_{10} 00110011_2 063_8 33_{16}

FORMAT: <00110011> < P1 > < P2 > < P3 >

P1-P2 = loop parameter
P3 = diagnostic section number

NO OP (COMPLEMENTARY)

FUNCTION: Causes the device to disregard the message byte.

OPCODE: 52_{10} 00110100_2 064_8 34_{16}

FORMAT: No variables or parameters

Table 2-1. Device Command Summary (continued)

DESCRIBE (GENERAL PURPOSE)

FUNCTION: Directs the device to return information about itself.

OPCODE: 53_{10} 00110101_2 065_8 35_{16}

FORMAT: No variables or parameters

INITIALIZE MEDIA (GENERAL PURPOSE)

FUNCTION: Initializes all the data fields of the currently selected unit.

OPCODE: 55_{10} 00110111_2 067_8 37_{16}

FORMAT: <00110111> <00000CWZ>$_{P1}$ < P2 >

P1 = initialize options byte

Options for disc media:
- CWZ = 000 Retain both factory (primary) and field (secondary) spares
- CWZ = 001 Retain factory spares only
- CWZ = 010 Retain no spares (for CE use only)

P2 = Block interleave byte

SET RPS (COMPLEMENTARY)

FUNCTION: Sets time-to-target and window-size time intervals for RPS data transfers. The command is accepted but the RPS function is not implemented.

OPCODE: 57_{10} 00111001_2 071_8 39_{16}

FORMAT: <00111001> < TIME 1 > < TIME 2 >

TIME 1 = time-to-target in hundreds of microseconds
TIME 2 = window size in hundreds of microseconds

Table 2-1. Device Command Summary (continued)

SET RETRY TIME (COMPLEMENTARY)

FUNCTION: Sets amount of time available for read and seek retries.

OPCODE: 58_{10} 00111010_2 072_8 $3A_{16}$

FORMAT: <00111010> < P1 > < P2 >

P1-P2 = retry time in tens of milliseconds (16-bit binary number)

SET RELEASE (COMPLEMENTARY)

FUNCTION: Defines how a device will respond to an internal release request.

OPCODE: 59_{10} 00111011_2 073_8 $3B_{16}$

FORMAT: <00111011> <TZ000000>

T = 1 Suppress release timeout
Z = 1 Release automatically during idle time

SET BURST (COMPLEMENTARY)

FUNCTION: Activates and deactivates burst mode.

OPCODE: 60_{10} 00111100_2 074_8 $3C_{16}$
61_{10} 00111101_2 075_8 $3D_{16}$

FORMAT: <0011110T> < P1 >

T = 0 Only the last burst is tagged with the message terminator (EOI on HP-IB)
T = 1 All bursts are tagged with the message terminator

P1 = Number of 256-byte segments in each burst (If P1=0, burst mode is deactivated.)

Table 2-1. Device Command Summary (continued)

SET STATUS MASK (COMPLEMENTARY)

FUNCTION: Provides selective masking of error conditions reported in the status message.

OPCODE: 62_{10} 00111110_2 076_8 $3E_{16}$

FORMAT: <00111110> < P1 > - - - - - - - - < P8 >

The bit positions in the parameter bytes (P1-P8) correspond to the bit positions in the status message. Refer to paragraph 2-45 in the CS/80 Programming Manual.

1 = masked error

SET VOLUME (COMPLEMENTARY)

FUNCTION: Selects a specific volume on the currently selected unit.

OPCODE: 64_{10} 01000000_2 100_8 40_{16}

FORMAT: <01000YYY>

YYY = volume number

SET RETURN ADDRESSING MODE (COMPLEMENTARY)

FUNCTION: Specifies the address format (single or 3-vector) returned in the parameter field of the status message.

OPCODE: 72_{10} 01001000_2 110_8 48_{16}

FORMAT: <01001000> <00000TTT>

TTT = addressing mode
000 = single-vector
001 = 3-vector

Table 2-2. Disc Drive Utilities

UTILITY OPCODE(S) ALLOWED(*) (hex)	MICRO OPCODE (hex)	UTILITY PERFORMED BY THE DISC DRIVE
32	C0	READ FULL SECTOR
32	C4	READ DRIVE TABLES
32	C5	READ RUN TIME DATA ERROR LOG
32	C6	READ ERROR RATE TEST DATA ERROR LOG
32	C7	READ FAULT LOG
30,32	C8	INITIATE PATTERN ERROR RATE TEST
30,32	C9	INITIATE READ ONLY ERROR RATE TEST
30,32	CB	INITIATE RANDOM ERROR RATE TEST
30,32	CC	INITIATE RANDOM READ ONLY ERROR RATE TEST
30	CD	CLEAR LOGS
30	CE	PRESET DEVICE
31	F6	WRITE SERIAL NO.
32	F6	READ SERIAL NO.
32	BF	SERVO TEST
32	F7	READ SEEK TIME

* OPCODE 30 executes utility with no message.
OPCODE 31 executes utility receive message.
OPCODE 32 executes utility send message.

2-6. GENERAL PURPOSE COMMANDS

This command group includes commands which allow the host to determine device type and operating characteristics or to ascertain storage media integrity. These commands are not considered "real time" commands and therefore should not be issued by the host unless it is willing to relinquish control of the drive for a varying period of time. General purpose commands are: locate and verify, spare block, release, release denied, describe, and initialize media.

2-7. DIAGNOSTIC COMMANDS

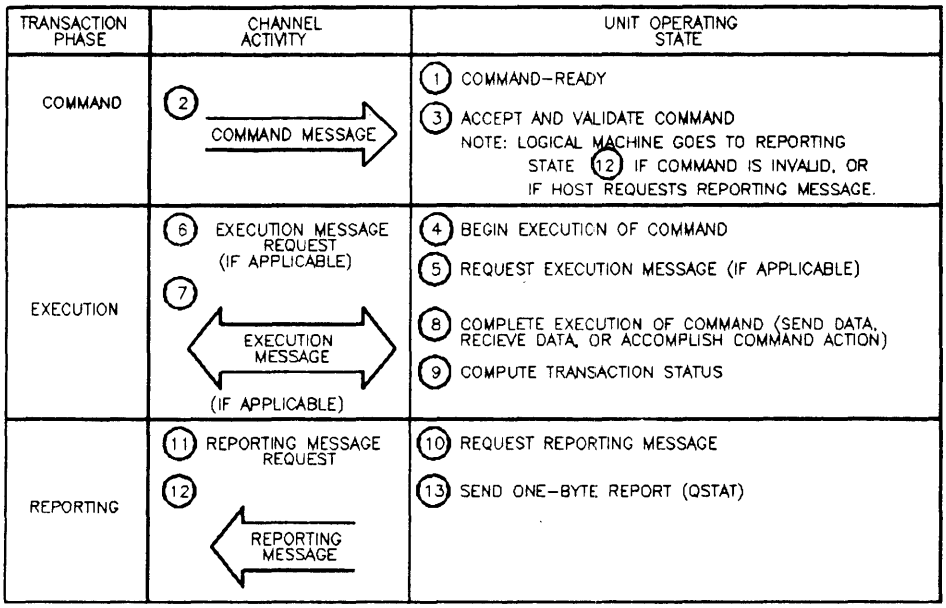
Diagnostic commands are intended to assist the host in isolating problems in the device to the replaceable assembly level. Some commands allow protected access to variables or data maintained by the device (such as error information), while others cause tests to be performed within the device, or on a specific area of the storage media. Diagnostic commands may be modified by complementary commands. Initialize diagnostic, initialize utility, and request status are all diagnostic commands.

2-8. TRANSPARENT MESSAGES

Transparent commands compensate for different types of channels and differences in operating environments. Transparent commands are intercepted by the device firmware and modify the normal command-execution-reporting transaction sequence. Transparent commands are explained in the *CS/80 Instruction Set Programming Manual*, part no. 5955-3442.

2-9. HEWLETT-PACKARD INTERFACE BUS

The Hewlett-Packard Interface Bus (HP-IB) provides a standardized method of connecting separate devices (see figure 2-2). The HP-IB permits transfer of commands and data between the components of a system on 16 signal lines. The interface functions for each system component are performed within the component so only passive cabling is needed to connect the system. The cable connects all controllers and other devices of the system in parallel.



(1) Logical Machine idle in command-ready state.

(2) Host sends command message.

(3) Logical Machine accepts and verifies command. If command is valid, Logical Machine moves to execution state. If not, Logical Machine moves to reporting state.

(4) Unit begins execution of command.

(5,6) If command involves data transfer, Logical Machine requests an execution message. If not, unit completes execution (6).

(7) Execution message is established if command involves a data transfer.

(8) Unit completes execution of command. If command involves data transfer, unit sends or receives data through channel module. If not, unit completes action called for in command message.

(9) Logical Machine computes completion status of transaction. Pass/Fail status is set into QSTAT, complete status set into request status.

(10,11) Logical Machine requests reporting message.

(12) Reporting message is established.

(13) Logical Machine sends 1-byte reporting message (QSTAT) indicting Pass/Fail status of transaction. Host must send request command for complete status report (20 bytes).

Figure 2-1. Transaction Structure

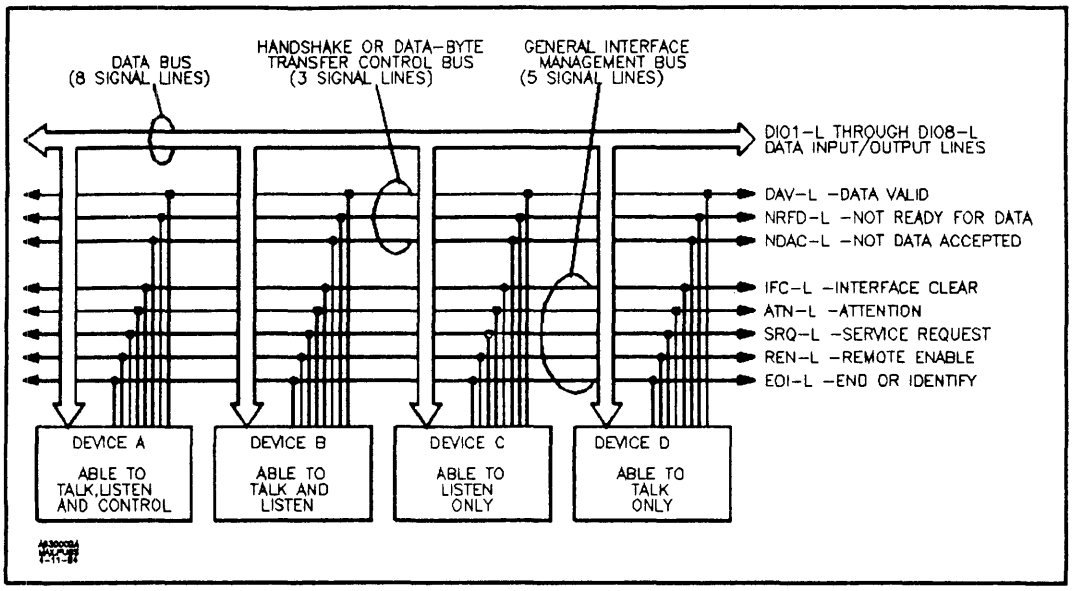


Figure 2-2. Hewlett-Packard Interface Bus Signal Lines

The Hewlett-Packard Interface Bus (HP-IB) has certain rules which must be followed for successful installation of the disc drive. Cabling is limited to 1 metre per HP-IB load. Typically the Central Processing Unit (CPU) is 7 equivalent loads and the disc drive is 1 equivalent load.

The CPU adheres to an HP standard which allows 7 metres of HP-IB cable between the CPU and the nearest device connected to it and 1 metre of cable between each additional device. The maximum configuration is eight devices (not including CPU) per HP-IB channel or a maximum of 15 metres or 15 equivalent loads.

The eight Data I/O lines are reserved for the transfer of commands, data, and other messages in a byte-serial, bit-parallel manner. Data and message transfers are asynchronous, coordinated by three handshake lines: Data Valid (DAV-L), Not Ready For Data (NRFD-L), and Not Data Accepted (NDAC-L). The other five lines are for bus management.

Information is transmitted on the data lines under sequential control of the three handshake lines (DAV-L, NRFD-L and NDAC-L). No step in the sequence can be initiated until the previous step has been completed. Information transfer can proceed as fast as devices can respond, but no faster than allowed by the slowest device presently addressed. This permits several devices to receive the same message byte concurrently.

Devices connected to the bus may be talkers, listeners, or controllers (refer to table 2-3). The Controller-In-Charge (CIC) dictates the role of each of the other devices by setting the Attention (ATN-L) line low and sending talk or listen addresses on the data lines. Addresses are set for each device at the time of system configuration. While the ATN-L line is low, all devices must listen to the data lines. When the ATN-L line is high, devices that have been addressed will send or receive data; all others ignore the data lines. Several listeners can be active simultaneously but only one talker can be active at a time. Whenever a talk address is put on the data lines (while ATN-L is low), all other talkers will be automatically unaddressed.

The Interface Clear (IFC-L) line places the interface system in a known quiescent state. The Remote Enable (REN-L) line is used to select between two alternate sources of device programming data such as the front panel or the HP-IB. The End Or Identify (EOI-L) line is used to indicate the end of a multiple-byte transfer sequence. In addition, when a controller-in-charge sets both the ATN-L and EOI-L lines low, each device capable of a parallel poll responds on the DIO line assigned to it.

Table 2-3. HP-IB Definitions

HP-IB TERM	DEFINITION	CONSIDERATIONS
TALKER	Any device which sends information over the HP-IB.	There can be only one TALKER sending information over the HP-IB at a time.
LISTENER	Any device which receives information over the HP-IB. Some devices can function as LISTENERS or TALKERS.	In a parallel poll system, there can be up to 8 LISTENERS receiving information over the HP-IB at the same time.
CONTROLLER	Any device that has been programmed to manage data flow between the TALKER and the LISTENER(s) in addition to being a TALKER and a LISTENER.	The CONTROLLER manages data flow by addressing one device as a TALKER and one or more devices as LISTENERS. There can be only one active CONTROLLER on the HP-IB at at any time. The active CONTROLLER is called the CONTROLLER-IN-CHARGE (CIC).
SYSTEM CONTROLLER	Any device that functions as a CONTROLLER and is able to gain absolute control of the HP-IB with the Interface Clear (IFC) signal.	There can be only one SYSTEM CONTROLLER connected to the HP-IB.

2-10. HP-IB COMMUNICATIONS

This section describes the formats and sequences for the HP-IB commands, messages, and transactions that occur between the Controller-In-Charge (CIC) and the disc drive. The following list explains the terms used in this section.

COMMAND -- A parcel of information transmitted over the channel (HP-IB) relating to a specific operation. Channel commands (usually a single byte) are used to manage operations on the interface channel. Device commands (usually more than one byte) are used to control the operation and are contained within the text of a command message.

UNIVERSAL COMMAND -- A channel command that causes all devices on the bus to perform a predetermined interface function. Refer to table 2-4.

PRIMARY COMMAND -- The primary I command is a channel command that begins the message sequence. It contains the command to listen or talk and the address of a particular device. The primary II command terminates the message with an unlisten or untalk command.

Table 2-4. Universal Command Formats

UNIVERSAL COMMAND	UNIVERSAL DEVICE CLEAR
ATN [P001CCCC] P=Parity Bit CCCC=Command Code	ATN [P0010100] P=Parity Bit

SECONDARY COMMAND -- The secondary command sets up the action required of the disc drive in the text of the message.

TEXT -- The text of the message can be 1 to n bytes depending on the required action. The

required action can be to receive further qualifying information or instructions (such as a device command), to receive write data, to send read or status data, or to perform a specific operation such as a CLEAR.

MESSAGE -- A unique sequence of command and text bytes transmitted over the channel during which the communication link between the devices (for example, CIC and the disc drive) remains unbroken.

COMMAND MESSAGE -- A single message containing all the information required to address a device and initiate an operation, set up a programmable parameter, or set up an operation to be executed by an execution message.

EXECUTION MESSAGE -- A single message containing all the information required to carry out an operation previously set up by a command message.

TRANSACTION -- A complete process or operation carried out over the channel. Some transactions are completed with only a command/report message, and some require a command, execution, and a reporting message.

2-11. CHANNEL MANAGEMENT

The following techniques are used by the CIC to manage the HP-IB: Parallel Poll and Universal Device Clear.

2-12. PARALLEL POLL. The CIC conducts a parallel poll on the HP-IB by asserting ATN-L and EOI-L simultaneously. Each device requiring service can then respond by asserting the DIO line corresponding to its address. The CIC then addresses only the device requiring service. If more than one device requires service, the CIC addresses the device with the highest priority (lowest address) first. Parallel Poll Enable (PPE) and Parallel Poll Disable (PPD) are internal states of the disc drive controller. PPE occurs when the disc drive requires service from the CIC. PPD is the opposite stat and occurs whenever the disc drive is active (for example, busy executing a command) or idle. A Parallel Poll Response (PPR) from the disc drive will occur if the CIC asserts both ATN-L and EOI-L and if the disc drive is in the PPE state.

2-13. UNIVERSAL DEVICE CLEAR. A universal command is a channel command that causes all devices on the HP-IB to perform a pre-determined interface function. Universal Device Clear erases information stored in the disc drive controller and places the disc drive in a known reset state. The universal device clear format is shown in table 2-4.

2-14. MESSAGE STRUCTURE

Each message contains the following components (refer to table 2-5).

-- Primary I Command
(unidirectional from CIC to device)

-- Secondary Command
(unidirectional from CIC to device)

-- Text (bidirectional)

-- Primary II Command
(unidirectional from CIC to device)

The CIC asserts ATN-L during primary and secondary commands to distinguish them from text information. The disc drive decodes the information contained in both the primary I and secondary commands to prepare for action specified in the text.

Table 2-5. HP-IB Message Structure

HEADER		TEXT	TRAILER
PRIMARY I	SECONDARY	DEVICE COMMAND OR DATA	PRIMARY II
[ATN] [ONE BYTE] --Unidirectional *CIC to device --Begins message *Addresses device to LISTEN or TALK *Universal	[ATN] [ONE BYTE] --Unidirectional *CIC to device --Set up device for further action	--Bidirectional --Qualifying instructions to device --Write data to device --Read data to CIC --Status data to CIC	[ATN] [ONE BYTE] --Unidirectional *CIC to device --Terminates message --Unaddresses device *Unlisten *Untalk

THEORY OF OPERATION

SECTION III

3-1. INTRODUCTION

The HP 7941 and HP 7945 Disc Drives are medium performance, random access, mass storage devices intended for use with small and medium sized computers. The formatted storage capacities of the HP 7941 and HP 7945 are 24 megabytes and 55 megabytes, respectively. In this section, "disc drive" refers to both the HP 7941 and 7945, unless otherwise specified.

The head-disc module in the disc drive is sealed and uses two (HP 7941) or four (HP 7945) 130-millimetre (5.12-inch) diameter nonremovable discs. One read/write head is used for each disc surface. The bottom surface of the lowest disc in the stack contains continuous prerecorded servo data which is used to ensure the precise positioning of the read/write heads.

The disc drive employs a peripheral mass storage structure which combines both host related functions and device (disc drive) related functions on to a single printed circuit assembly. In this single board controller (SBC) structure, the host related functions are controlled by specific host dependent controller (HDC) circuitry and microprocessor code, and the device related functions are controlled by specific device dependent controller (DDC) circuitry and microprocessor code.

Common host functions include: host interface, direct memory access (DMA), error correction, control for device dependent execution of commands, status monitoring, and diagnostic self-test routines.

The device dependent functions include all data stream manipulations necessary to read or write data on the disc. Functions include serialization/deserialization, modified frequency modulation (MFM) encoding/decoding, DMA hand shaking, and error detection.

Associated with the SBC device dependent functions is a disc drive assembly which contains a sealed head-disc module and electronic control and read/write circuits. The circuits, operating with the SBC device dependent circuits, maintain the read write heads over the desired track, maintain precise disc rotational speed, and perform read and write operations.

The SBC communicates with its host computer over the Hewlett-Packard Interface Bus (HP-IB). The SBC communicates with the disc drive assembly (HDA), via the data and control lines of the ST506-Interface. The ST-506 Interface is an electrical and mechanical standard for disc drives established by the Shugart Corporation and adapted as an industry-wide standard.

The disc drive consist of single-board controller (SBC) printed circuit assembly (PCA) A5, disc drive assembly A1, and power supply assembly PCA-A4. Disc drive assembly A1 and power supply assembly PCA-A4 are mounted side by side at the bottom of the cabinet. SBC assembly PCA-A5 is mounted horizontally above PCA-A1 and PCA-A4. In this configuration assemblies A2 and A3 are unassigned.

Circuits on the single-board controller (SBC) PCA-A5 include:

- HP-IB interface integrated circuit (IC)
- a microprocessor
- firmware in erasable programmable read-only memory (ROM)
- random access read/write memory (RAM)
- a custom designed DMA gate array IC
- self-test switches and display
- a disc controller IC
- a phase-lock loop (PLL) IC.

Circuits on the disc drive assembly PCA-A1 include:

- a sealed head disc module with spindle motor
- discs
- read/write (R/W) heads
- a servo head
- read preamplifer/writer driver IC's
- servo preamplifer IC
- rotary voice coil head positioning mechanism (actuator)
- air filtration components
- a microprocessor
- a programmed logic array (PLA)

- a read/write data channel
- circuits for actuator servo control and spindle speed control

Power supply assembly PCA-A4 is a self-contained switch-mode power supply which supplies dc voltages and a power-on reset signal to the disc drive.

A typical operation of the disc drive, locate and read, is performed as follows: The locate and read command from the host computer enters the SBC HP-IB interface IC, is stored in RAM, and interpreted by the SBC microprocessor. The SBC microprocessor executes from the executive (EXEC) firmware in ROM to carry out its control and management functions. The EXEC code in ROM directs the DDC code in ROM to execute commands necessary for command completion. The DDC ROM firmware controls disc drive assembly PCA-A1 via the SBC device dependent circuits.

The device dependent circuits are given the seek argument, which cause the disc controller IC to drive the actuator servo control in disc drive assembly PCA-A1 via its microprocessor and PLA with a stream of pulses which represent the seek offset argument. Once on track; the SBC device dependent circuits verify the locality from information on the data track. If the head is on the proper track, the disc rotates until the correct section is read. The MFM encoded serial data stream from the disc passes from the read/write head through the read preamplifier/ write driver IC and the read/write data channel to the SBC PPL IC and disc controller IC. Here the MFM data is decoded and packed into bytes. These bytes are sent to the SBC RAM, under control of the DMA gate array IC. As data is being assemblied, it is checked, one sector at a time, for errors. Errors are corrected using information supplied by the disc controller IC. The SBC exec firmware coordinates the transfer of data from the RAM to the host computer via the DMA gate array IC and the HP-IB interface IC.

The operation continues until the requested amount of data has been successfully read, assembled, checked for errors, buffered in RAM, and sent to the host computer. When the data transfer is complete, the SBC circuits give ending status to the host computer.

A locate and write operation is similar to the locate and read operation previously described except for the direction in which the user data flows. The set up and head positioning operations are the same. However, the data is accepted into the RAM from the HP-IB interface IC prior to the seek and verify operation. This is done to allow the data to start moving from the RAM through the SBC disc controller IC serializer and formatter, and the disc drive read/write channel as quickly as possible once it is determined that the head is in the proper position.

Included in the SBC firmware are diagnostic self-test routines which exercise key functions of the disc drive and indicate faults on a 2-digit hexadecimal display which is visible through an opening in the rear panel of the disc drive. Also, a front panel FAULT/ON LINE indicator driven by SBC PCA-A5 shows the operating status of the drive. The disc drive has dedicated maintenance tracks where the results of some of the self tests are logged. The internal diagnostics permit off-line testing of the SBC, disc drive assembly, and power supply. This furnishes a quick and easy means of fault isolation to the unit, assembly, and subtest level. An additional troubleshooting aid is provided by a CS/80 External Exerciser which links the disc drive internal diagnostics and utility programs to service-trained personnel. The CS/80 External Exerciser can also be used to check the HP-IB channel and the interaction of the disc drive with the system host.

The disc drive circuitry is discussed in this section, first at a basic block diagram level and then at a more detailed functional block diagram level. A description of the disc recording format is also provided.

In order to facilitate text references to the three sheets of the functional block diagram (figure 3-4), each sheet is identified by a large numeral in the lower right-hand corner of the page. These numerals are printed in boxed characters in the text, for example: **1B** .

The mnemonics used in the functional block diagram and accompanying text to identify analog and digital signals are defined in table 3-1. In the "Source" column of table 3-1, the assembly where the signal originates is listed , followed by a boxed numeral identifying the sheet of the functional block diagram where the assembly is shown.

Most of the mnemonics listed in table 3-1 have "-L" or "-H" suffixes. These suffixes identify active low or active high logic signals, respectively. Signals without such suffixes are usually bus or analog signals.

In addition, section IV, Service Information, contains system cabling and signal distribution diagrams for the disc drive.

3-2. DISC FORMAT

The two plated metal discs in disc drive assembly A1 (HP 7941) provide three data surfaces, each with one read/write head. The fourth surface is used with a servo head for prerecorded servo data. The four discs in the HP 7945 provide seven data surfaces and one servo surface. See figure 1C.

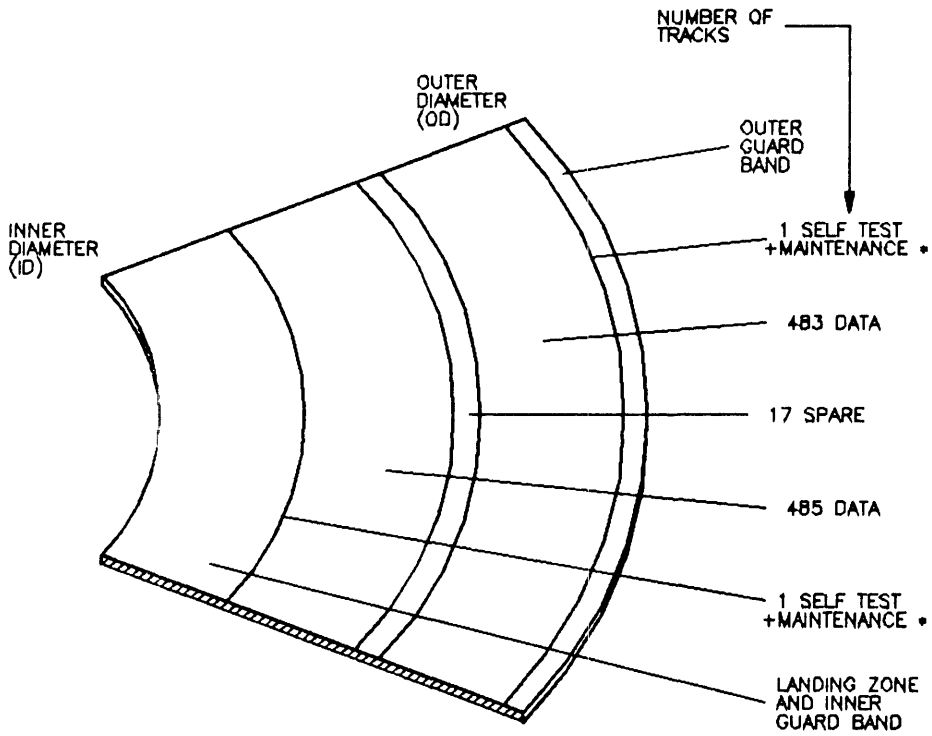
Each data surface is divided into 987 concentric circles called tracks. See figure 3-1. From the outside diameter of the disc there are: one self-test/maintenance track, 483 data tracks, 17 spare tracks, 485 data tracks, and one self-test/maintenance track.

The two self test/maintenance tracks are used for testing reading and writing. These tracks also contain service information, including run time logs, fault logs, and a spare table directory. See figure 3-1. The self test/maintenance tracks are located at the inner diameter (ID) and outer diameter (OD) of the disc to permit read/write testing at these locations. Also, duplicating the service information at two locations reduces the possibility of loss of data due to recording medium failure. The 968 data tracks are used for reading and writing data. This provides the user with 968 addressable cylinders. The 17 spare tracks are used for sparing out tracks containing hard errors.

Each data track is organized into smaller sequentially-numbered blocks of data called sectors. Figure 3-2 shows the track format, based on 32 data sectors, each having 256 bytes of data information. The beginning of each sector is identified by a prewritten identification (ID) field which contains the physical sector address plus cylinder and head information. This ID field is followed by the data field. The beginning of both the ID field and the data field is flagged by unique two-byte characters called address marks. The first byte in both address marks is a hexadecimal A1 pattern. This is followed by a FE pattern for the ID address mark and an F8 pattern for the data address mark.

A summary of the recording capacity provided by user available data tracks in the HP 7941 and HP 7945 is provided below.

	Data Bytes Per	Sectors Per	Tracks Per	Heads Per
Sector	256			
Track	8,129	32		
Head	7,929,856	30,976	968	
7941	23,789,568	92,928	2,904	3
7945	55,508,992	216,832	6,776	7



*SELF TEST AND MAINTENANCE TRACK CONTENTS:

SECTOR ADDRESS	OUTER DIAMETER (OD)	INNER DIAMETER (ID)
0	PRODUCT NO.	SERIAL NO.
1-5	RUN TIME LOG	RUN TIME LOG
6-10	ERROR RATE TEST (ERT) LOG	ERROR RATE TEST (ERT) LOG
11-15	FAULT LOG	FAULT LOG
16-18	SPARE TABLE	SPARE TABLE
19-20	SELF TEST LOCATION	SELF TEST LOCATION
21-22	SELF TEST LOCATION	SELF TEST LOCATION
23-31	NOT USED	NOT USED

FILE=FSJEF12A

Figure 3-1. Disc Recording Format

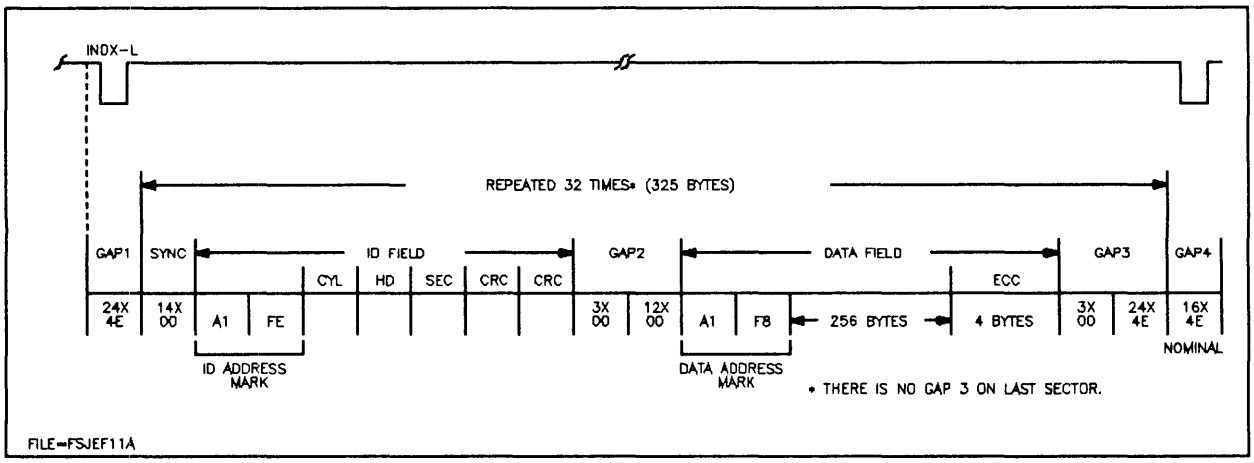


Figure 3-2. Track Recording Format

3-3. SBC PCA-A5

The single-board controller (SBC) PCA-A5 provides two functions: interface between the host computer (host dependent functions) and interface to the disc drive assembly PCA-A1 (device dependent functions). The host dependent interface is accomplished via the HP-IB and the device dependent functions are handled via the ST-506 interface.

Host dependent functions include:

- Host interface via the HP-IB.
- Direct memory access (DMA) capability.
- A random access memory (RAM) buffer for data examination for integrity, error correction, and speed matching between devices.
- Firmware for a microprocessor to execute DDC (disc drive) commands and monitor status.
- Self-test diagnostic capabilities.

Device dependent functions include:

- Accepts disc drive control commands and provides high-level status commands.
- Executes the disc drive commands by transferring them into ST-506 interface control sequencer.
- Performs all of the manipulations of the data stream necessary to read or write data on the disc. Functions required for this manipulation include serialization/deserialization, MFM encoding/decoding, error detection, DMA data transfer handshaking, and write precompensation.

The firmware in the SBC consists of two segments. One segment is the executive operating system (EXEC ROM) which controls resource allocation (including the DMA gate array IC and RAM), and the passing of messages between the DDC firmware and the host interface firmware. The remaining segment (DDC ROM) handles the control firmware for the disc drive. Each set of firmware takes care of its own tasks, performing whatever function the host or disc drive has requested. Self test firmware is included in each of the two segments.

The following paragraphs provide a more detailed description of the host dependent controller circuitry, as shown on the disc drive functional block diagram, sheet 1A. Refer to table 3-1 for a description of the mnemonics used in the text and on sheet 1A.

3-4. SBC INTERNAL BUS ARCHITECTURE

The internal bus architecture of the SBC for host dependent functions consists of the following buses:

- HP-IB Data Bus
- RAM Data Bus
- Microprocessor Address Bus

- Microprocessor Data Bus
- DMA Gate Array Data Bus
- Read/Write Data Bus

A brief description of the function of each internal bus is provided in the following paragraphs.

3-5. HP-IB DATA BUS. The HP-IB Data Bus is accessed by the microprocessor and by the DMA gate array IC input and output processes. The microprocessor must read and write to the various registers in the HP-IB interface IC in order to prepare for data transfers to and from the host computer. Buffers separate the HP-IB Data Bus from the RAM Data Bus and permit speed matching between the HP-IB data rate and the DMA gate array IC data transfer rate.

3-6. RAM DATA BUS. The RAM Data Bus is used for all data transfers between the RAM and the microprocessor, the RAM and the device dependent circuits, and the RAM and the HP-IB. The use of the RAM is time multiplexed , so that in one half of the microprocessor clock cycle, the microprocessor has access to the RAM, and in the other half, the DMA gate array IC has access to the RAM.

3-7. MICROPROCESSOR ADDRESS BUS. The Microprocessor Address Bus points to the next instruction or data source. The circuits addressed by the Microprocessor Address Bus include the HP-IB interface IC, RAM (via the address multiplexer), DMA gate array IC, EXEC ROM, and the DDC ROM. The microprocessor can write directly to the device dependent circuits via a buffer and the Control/Status Address Bus to operate the mass storage unit.

3-8. MICROPROCESSOR DATA BUS. The Microprocessor Data Bus interconnects the microprocessor, the EXEC ROM, and the DDC ROM. The microprocessor RAM exists on a separate bus so that the RAM can be shared by the microprocessor and the DMA gate array IC. The bidirectional data on the Microprocessor Data Bus includes preprogrammed control sequences (algorithms) in ROM and control/status information from the device dependent circuits. The Microprocessor Data Bus is connected to the device dependent circuits via a bidirectional buffer and the Control/Status Data Bus.

3-9. DMA GATE ARRAY DATA BUS. The DMA Gate Array Data Bus is used when the microprocessor must read or write to registers in the DMA gate array IC, including the DMA registers. EXEC and DDC operations.

3-10. READ/WRITE DATA BUS. The Read/Write Data Bus is used to pass data to and from the device dependent circuits. The bus becomes the Read/Write Data Bus linking the host dependent circuits and the device dependent circuits.

The Read/Write Data Bus is the path taken by all the data which flows between the host computer and the device dependent circuits. Details of these signals, and their associated select and strobe lines are given in the following paragraphs.

The Read/Write Data Bus and the Control Status Data Bus provides the communication link between the SBC host dependent circuits and device dependent circuits.

The Control/Status Data Bus is used to send commands to the device dependent circuits such that it can initiate the transfer of information to or from the recording medium, or it can be used to interrogate the status of the device dependent circuits and its drive mechanism. A Control/Status Address Bus associated with the Control/Status Data Bus provides an addressing capability.

3-11. CONTROL/STATUS DATA BUS. Control/Status Data Bus, Bits CSB0-H through CSB7-H comprise a bidirectional 8-bit data bus which is used to pass control and status information between the host dependent circuits and device dependent circuits.

3-12. CONTROL/STATUS READ STROBE. Control/Status Read Strobe signal CSRS-L is used to pass bytes to the SBC across the Control/Status Data Bus. These bytes will be of a status nature since the actual recording medium information will be passed over the Read/Write Data Bus.

3-13. CONTROL/STATUS WRITE STROBE. Control/Status Write Strobe signal CSWS-L is used to pass bytes from the host dependent circuits to the device dependent circuits across the Control/Status Data Bus.

3-14. CONTROL/STATUS ADDRESS BUS. Control/Status Address Bus, Bits CSA0-H through CSA5-H are the address lines associated with the Control/Status Data Bus. The address lines are used to access specific registers in the device dependent circuits.

3-15. READ/WRITE DATA BUS. Read/Write Data Bus, Bits DATA0-H through DATA7-H comprise an 8-bit bus used to pass high-speed data between the host dependent circuits to the device dependent circuits. The data on the bus is the digital information going to and coming from the recording medium.

3-16. DATA REQUEST IN/DATA REQUEST OUT. Data Request In signal DRIN-L and Data Request Out signal DROUT-L are DMA request lines used to transfer bytes over Read/Write Data Bus DATA0-H through DATA7-H. The "out" direction is defined as being from the SBC to the host dependent circuits or to the device dependent circuits.

3-17. DATA STROBE IN/DATA STROBE OUT. Data Strobe In signal DSIN-L and Data Strobe Out signal DSOUT-L are SBC-generated DMA strobe lines which accompany the transferring of data between the host dependent circuits or to device dependent cirsuits.

3-18. HP-IB INTERFACE IC

The HP-IB interface integrated circuit is a talker/listener device. This IC provides the interface between the host data channel (HP-IB) and the mass storage device. The IC is accessed by the microprocessor and by the DMA gate array IC input and output processes. The microprocessor must read and write to the various registers in the HP-IB interface IC in order to prepare for data transfers to and from the host computer. Buffers separate the HP-IB data bus from the RAM data bus.

The HP-IB interface IC implements all of the talker/listener functions of the HP-IB including data transfers, handshake protocol, talker/listener addressing, service request, and serial and parallel polling. HP-IB signals connected to the IC include HP-IB Data I/O Bus DIO1-L through DIO8-L, End or Identify EOI-L, Data Valid DAV-L, Not Ready for Data NRFD-L, Not Data Accepted NDAC-L, Interface Clear IFC-L, Attention ATL-L, Service Request SRQ-L, and Remote Enable REN-L. The functions of these signals are described in table 3-1.

3-19. MICROPROCESSOR

The microprocessor provides overall control of all device functions. The host dependent controller employs an internal 8-bit microprocessor. Firmware associated with the microprocessor includes the EXEC ROM and the DDC ROM. The EXEC ROM and the DDC ROM provide approximately 44 kilobytes of code.

3-20. HP-IB ADDRESS SWITCH

The HP-IB ADDRESS switch is a 4-segment switch which is accessible to the operator through an opening on the rear panel of the disc drive. Three of the segments allow an HP-IB device address in the range of 0 through 7 to be set. The fourth segment on the switch is not used.

3-21. CHANNEL STATUS

The channel status block provides the microprocessor with information regarding the current status of the DMA gate array IC (DMA full, DMA not full) and details of the unit connected to the SBC.

3-22. SELF-TEST SWITCHES

Two momentary contact pushbutton switches, accessible through openings in the rear panel of the disc drive, allow the operator to initiate operation of the internal self-test diagnostic routines. One switch, labeled SELF TEST, initiates the self-test routines. The other switch, labeled DISPLAY RESULTS, causes the self-test results to be displayed on the self-test display. The microprocessor can read the operation of the switches and will initiate the appropriate self-test operations.

3-23. SELF-TEST DISPLAY

The Self-Test display consists of two 7-segment LED's which are visible through openings in the rear panel of the disc drive. The display is controlled by the microprocessor and provides a 2-digit hexadecimal readout of self-test results, including the defective unit, field replaceable assembly (FRA), and subtest failure number. Information on

how to interpret the self-test readout is contained in section IV, Service Information.

3-24. DMA GATE ARRAY IC

The DMA (direct memory access) gate array IC is a custom-designed integrated circuit which performs the DMA function for the host dependent controller. DMA is defined as the ability to perform complete memory cycles without the intervention of the SBC microprocessor. The DMA gate array IC controls data transfers between the host and RAM. It also transfers self-test status information from the microprocessor to the self-test display. The DMA gate array is set up for either an input to or an output from the RAM. Once activated, the DMA gate array IC performs reads or writes to the RAM completely transparent to the microprocessor.

3-25. RAM

The random access memory (RAM) is a temporary storage location for all data transfers. The use of RAM is time multiplexed, so that for one half of a microprocessor clock cycle, the microprocessor has access to RAM; for the other half, the DMA gate array IC has access to RAM.

3-26. EXEC ROM

The executive (EXEC) ROM contains the firmware which controls operation of the SBC microprocessor and the interface with the host computer. This includes decoding and validating host commands, and setting up the data transfer paths. The EXEC ROM employs a 16k by 8 ROM. All 16k is used.

3-27. DDC ROM

The device dependent (DDC) ROM contains firmware which provides permanent storage for the preprogrammed sequences which govern operation of the device dependent circuits. The ROM is addressed by the Microprocessor Address Bus and information is sent out over the Microprocessor Data Bus. The DDC ROM employs one ROM.

3-28. ADDRESS MULTIPLEXER

The address multiplexer (MUX) allows the RAM addresses to be multiplexed between the microprocessor and the DMA gate array IC.

3-29. CLOCKS AND CONTROL LOGIC

The clocks and control logic block contains all of the circuitry controlling the timing and operation of the host dependent controller.

3-30. BUFFERS

The buffers consist of a number of unidirectional and bidirectional buffers which provide the required communication and isolation between the various buses of the SBC. On sheet 1A, unidirectional buffers are identified by a single arrow and the bidirectional buffers by dual arrows.

3-31. TYPICAL HOST DEPENDENT TRANSACTION

The following is a description of a typical host dependent transaction -- the flow of data between the host computer and the disc drive. To start the process, the host computer sends a command to the disc drive asking for the transfer of a sector of information to the host. The command is received by the SBC executive firmware and the command is validated. The command is then passed to the disc drive DDC ROM in the form of a message. The message is received and the disc drive firmware issues seek and read commands to its device dependent servo and read/write circuitry. Also, the disc drive firmware requests from the executive firmware an input channel to the DMA gate array IC and a buffer in RAM. When allowed to do so, the disc drive firmware programs the DMA gate array IC for an input transfer. In conjunction with this action, a request is made to the executive firmware for the use of the DMA gate array IC output channel, which will transfer data from RAM to the HP-IB interface IC.

When a RAM buffer is full of data from the disc, the buffer is given the process that will output the buffer to the HP-IB interface, with the executive firmware starting the buffer transfer. Multiple buffers may be transferred. The DMA gate array IC transfers the data from the RAM to the host computer and terminates the operation when the buffer is empty. The host computer interrogates the SBC as to the status of the transfer, which the SBC returns to the host. This completes the host computer's request for disc information.

The following paragraphs provide a more detailed description of the device dependent controller circuitry, as shown on the disc drive functional block diagram, sheet 1B. Refer to table 3-1 for a description of the mnemonics used in the text and on figure 1B.

3-32. HOST DEPENDENT TO DEVICE DEPENDENT COMMUNICATIONS

Communication between the host dependent circuits and device dependent circuits takes place via the three primary buses for passing control/status information and data to be stored or retrieved. These are:

- Control/Status Data Bus
- Control/Status Address Bus
- Read/Write Data Bus

A brief description of the function of each bus, as related to the operation of the device dependent circuits, is provided in the following paragraphs.

3-33. CONTROL/STATUS DATA AND ADDRESS BUSES. All disc drive high-level control commands and status information are passed to/from the device dependent circuits via Control/Status Data Bus, Bits CSB0-H through CSB7-H and Control/Status Address Bus, Bits CSA0-H through CSA5-H. Control and status information ultimately resides in specific registers in the device dependent circuits. The Control/Status Address Bus is a unidirectional bus since it passes only address information. The actual values sent or received from a register are sent over the Control/Status Data Bus. This bus is a bidirectional bus since data can be sent or received over it.

To send control/status information to the device dependent circuits, the target register is addressed with the Control/Status Address Bus, the data to be written to the register is placed on the Control/Status Data Bus, Select signal SEL-L is set low, and Control/Status Write Strobe CSWS-L is pulsed.

To retrieve information, the target register is addressed with the Control/Status Address Bus, Select signal SEL-L is set low, and Control/Status Read Strobe CSRS-L is pulsed. As CSRS-L is pulsed, the register value is placed on the Control/Status Data Bus.

3-34. READ/WRITE DATA BUS. Disc storage data to be stored or retrieved is passed over Read/Write Data Bus DATA0-H through DATA7-H. When a command requires data to be transferred, the data is passed on the Read/Write Data Bus, one byte at a time, and clocked in or out using the appropriate DMA handshake lines DRIN-L, DSIN-L, DROUT-L, or DSOUT-L.

When writing data to the disc, the SBC places the first byte of the transfer on the Read/Write Data Bus. However, the actual transfer of data does not begin until the device dependent circuits are ready to accept data (that is, the disc has arrived at the target sector). When ready to accept data, the device dependent circuits activates Data Request Out line DROUT-L. When the SBC senses DROUT-L, it pulses Data Strobe Out line DSOUT-L, clocking the byte out from the host dependent circuits onto the Read/Write Data Bus. This DROUT-L/DSOUT-L handshake continues until the transfer length determined by the sector count register in the disc controller IC has been satisfied.

When reading data from the disc, the Data Request In DRIN-L and Data Strobe In DSIN-L lines are used to handshake data into the host dependent circuits from the device dependent circuits.

In both the write and read operations described above, the Data Request lines signal the readiness of the device dependent circuits to transfer a byte. Data Strobe lines are activated by the host dependent circuits to clock data in or out.

3-35. RECEIVER/DRIVER. The receiver and driver used to provide a bidirectional data transmission path for Read/Write Data Bus DATA0-H through DATA7-H between the device dependent circuits and host dependent circuits consist of two identical octal D-type flip-flop devices with 3-state outputs. The receiver used for unidirectional input of Control/Status Address Bus CSA0-H through SCA5-H and Select line SEL-L consists of an octal buffer/line driver with 3-state outputs.

3-36. TRANSCEIVER The transceiver is used to manage control status information to the disc controller IC and disc data which passes through the disc controller IC.

3-37. SBC/DISC DRIVE A1 COMMUNICATION

Communication between the SBC and disc drive assembly A1 takes place via the ST-506 Interface. This function is provided primarily by the disc controller IC and some additional support circuits.

The ST-506 Interface signals are divided into two groups -- control and data. Signals in the control group include Head Select Bits HS0-L through HS8-L, Seek Complete SKCMP-L, Track 0 TRK0-L, Write Fault WFLT-L, Index INDX-L, Ready RDY-L, Step STEP-L, Direction DIR-L, Write Gate WGATE-L, and Drive Select Bit DS0-L.

Signals in the data group are differential MFM Write Data lines WMFM+, WMFM- and differential MFM Read Data lines RMFM+, RMFM-.

The functions of the ST-506 Interface control and data signals are described in table 3-1, List of Mnemonics.

3-38. CONTROLLER IC AND REGISTER DECODE LOGIC

The controller IC and register decode logic controls selection of the disc controller IC and a number of registers external to the disc controller which provide additional control, management, and status functions. Inputs to the decode logic are Control/Status Address Bus, Bits CSA0-H through CSA5-H, Control/Status Read Strobe CSRS-L, Control/ Status Write Strobe CSWS-L and Select line SEL-L. The registers controlled by the decode logic include four general purpose registers, and two test registers. Details of these components are provided in the following paragraphs.

3-39. SELF-TEST REGISTER. A general-purpose read-only register which contains self-test information.

3-40. GPC REGISTER. A general-purpose write-only register which performs hardware control functions. The register provides drive for the front panel FAULT/ON LINE indicator via outputs RED-L and GREEN-L.

3-41. DDC ERRORS REGISTER. A general-purpose read register which contains device dependent error/fault descriptions and DMA data transfer information.

3-42. PUPO REGISTER. A general-purpose read/write register which acts as an overflow for DMA data transfer sector counting. The mnemonic PUPO represents Protect Under/Protect Over.

3-43. DISC CONTROLLER IC

The disc controller IC is a single-chip IC which provides most of the control signals to manage the ST-506 Interface. To perform disc storage functions, command information is written into registers in the disc controller via the Control/Status Interface Bus. At the end of the command, the disc controller carries out the command by manipulating the ST-506 Interface and the DMA control lines, as needed. Operation of the disc drive begins when the SBC initiates a command by loading the internal registers in the disc controller. Information such as cylinder, sector, and head number is written to these registers with the selected address lines. The disc controller is run by an internal programmed logic array (PLA) which controls the flow of data through the chip, recognizing the commands and formatting the data.

During a write operation, parallel data is read from the Read/Write Data Bus and written to a specific sector. However, before the write operation can begin, the cylinder and sector must be located. The disc controller consults its internal cylinder position information and compares it with the requested cylinder number. If necessary, a seek is performed to position the head over the desired track. After the disc controller finds an ID field which matches the cylinder, head, and sector, the disc controller reads parallel data in from the Read/Write Data Bus, serializes it, converts it into an MFM format, and sends it to the ST-506 Interface to be written on the disc. If the original command specified multiple sectors, the next logical sector must be searched for and the process is repeated. After the last sector is written, the disc controller returns the bus back to the SBC.

The read operation is similar to the write operation, except that decoded data is sent out on the Read/Write Data Bus and written into RAM in the SBC. MFM-encoded read data is entered into

the disc controller over the differential RMFM+, RMFM-lines together with a synchronous clock generated by the external phase-locked loop IC.

The controller includes error correction code (ECC) logic which provides data error detection capabilities and in addition, can support data error corrections. This function provides the capability to detect errors of up to five consecutive bits in length anywhere within a full sector.

The disc controller computes four ECC bytes for each sector and appends these bytes to the end of each data field during sector write operations. During sector reads, the disc controller computes four error syndrome bytes. These error syndrome bytes are then used to compute correction information if an error occurs.

Error detection is signaled when an error control line in the logic goes active. This error status line runs to the DDC errors register. Host firmware can recognize a data error by examining bit 5 of the DDC errors register.

Error correction is performed by using information supplied by the disc controller. When a data error arises, the disc controller makes information available to the SBC that tells a) the location of the error within the sector (error offset), and b) the error pattern required for correction. The exec firmware uses this information to correct data errors within the target sector.

The ECC function can be operated in a standard "generation" mode or in a "long" mode. In the "generation" mode, the ECC bytes are generated by the disc controller and applied to the data field during sector writes. Also, syndrome bytes are stored in the disc controller for subsequent reading upon detection of a data error. In the "long" mode, ECC or syndrome bytes are not generated by the disc controller. Instead, the user can issue four bytes to be appended on a sector during writes. In the "long" mode, the four bytes following the data field are passed directly back to the user and are not used for syndrome generation. The "long" mode is employed for diagnostic checkout of the ECC hardware and firmware; it is not used during normal operation of the disc drive.

3-44. PHASE-LOCKED LOOP IC

The data separation function of the disc controller IC is implemented with a phase-locked loop (PLL) IC. The PLL separates the clock and data pulses contained in the raw MFM-encoded read data signal. This signal, received from the read chain in disc drive assembly A1, is labeled RMFM+, RMFM-. The PLL IC passes synchronized data and a read clock to the disc controller IC where the actual data separation and byte packing takes place.

3-45. LATCH

The latch is an octal D-type flip-flop which latches in head and disc drive information which is supplied to the ST-506 Interface. This latch is necessary since the disc controller IC does not supply these signals. Outputs are Drive Select line DS0-L and Head Select signals HS0-L through HS8-L.

3-46. DMA HANDSHAKE CONTROL

The DMA control logic includes the circuits needed to: interface with the DMA operation; supply Data Request signals DRIN-L, DROUT-L; and accept Data Strobe signals DSIN-L, DSOUT-L. Disc data is transferred to/from the disc one byte at a time via the drivers and receivers on Read/Write Data Bus DATA0-H through DATA7-H.

3-47. CLOCK GENERATOR

The clock generator supplies a 5-MHz clock signal to the disc controller IC to synchronize write operations. The generator also provides a 10-MHz clock input to the phase-locked loop IC in the data separator circuit.

3-48. DISC DRIVE A1

Disc drive assembly A1 consists of a sealed head-disc module containing a rotary voice-coil head positioning mechanism (actuator), recording medium, read/write heads, a servo head, a spindle motor, and air filtration components. Also included in assembly A1, external to the head-disc module, are two PCA's which contain read/write, servo, and interface control electronics.

The components in disc drive assembly A1 perform the following functions:

- Perform a power-on self-test.
- Interpret and generate control signals.
- Position and maintain the read/write heads over the desired track.
- Maintain precise disc rotation speed.
- Read and write MFM-encoded data.
- Report write faults.
- Provide a contamination free environment for the actuator, recording medium, and heads.

The electronics are packaged on two PCA's. The outermost PCA on the assembly, to which the ST-506 control and data signals are connected, includes: read/write circuits, interface drivers and receivers, microprocessor control logic, write fault detection, drive selection, and an index circuit.

The second PCA, mounted under the outermost PCA, accepts +5V from power supply assembly A4 and performs the following functions: spindle speed control, head actuator positioning, track 0 detection, power reset, and clock generation.

Interpretation and generation of control signals are performed by a microprocessor and a programmable logic array (PLA). Positioning of the heads is achieved by driving the actuator with a dedicated track-following servo system. Speed control of the spindle motor is performed by a phase-controlled driver circuit using a 360-Hz reference signal. MFM-encoded data is written to and read from the discs by means of a read/write data channel. Write errors are reported by read preamplifier/write driver IC's in the read/write data channel. Contamination protection for the heads, actuator, and recording medium is achieved by enclosing these components in a sealed head-disc module having a built-in air filter.

The following paragraphs provide a more detailed description of the disc drive assembly A1 components and electronic circuits, as shown in the disc drive functional block diagram, sheet 1C. Refer to table 3-1 for a description of the mnemonics used in the text and sheet 1C.

3-49. DISC DRIVE A1/SBC CONTROL COMMUNICATION

The ST-506 Interface control signals input to disc drive assembly A1 via input buffers are Step STEP-L, Drive Select DS0-L, Head Select HS0-L through HS8-L, Direction DIR-L, and Write Gate WGATE-L. These signals are applied to either the microprocessor or the PLA, as shown in sheet 1C

The ST-506 Interface control signals output from disc drive assembly A1 via output drivers are Seek Complete SKCMP-L, Track 0 TRK0-L, Write Fault WFLT-L, and Ready RDY-L. The majority of these signals are output by the microprocessor or the PLA. See sheet 1C.

Head Select lines HS0-L through HS8-L are applied via input buffers directly to head select and control logic which outputs Chip Enable signal CE, Write Select WS, and Head /Select lines HS1-H, HS2-H, to the read preamplifier/write driver IC's in the sealed head-disc module.

3-50. INPUT BUFFERS

The ST-506 Interface control signals from the device dependent circuits are input to the microprocessor and the PLA via input buffers.

3-51. OUTPUT DRIVERS

The ST-506 control signals from disc drive assembly A1 are output via open-collector drivers. Each driver is capable of sinking 48 milliamperes at its low level (true state) with a maximum of 0.4 volts measured at the driver. When the driver is in its high level (false state), the driver transistor is off. The output control signals are gated by a Drive Select line developed from the Drive Select input DS0-L.

3-52. DISC DRIVE A1/SBC DATA COMMUNICATION

Data signals passed between disc drive assembly A1 and the SBC are passed over the ST-506 Interface data lines. MFM Read Data signals RMFM+, RMFM- from the read/write data channel in A1 are output to the SBC via a differential line driver. MFM Write Data signals WMFM+, WMFM- from the SBC are input to the A1 read/write data channel via a line receiver.

3-53. MICROPROCESSOR AND PLA

Disc drive assembly A1 employs a microprocessor and a programmed logic array (PLA) to control its internal operations. These devices receive commands from the device dependent controller over the control lines of the ST-506 Interface bus. These operations include servo control, spindle speed control, read/write, and error/fault reporting.

The microprocessor consists of a single chip microcomputer IC which incorporates an 8-bit central processing unit (CPU), 4 kilobytes of program memory (ROM), 256 bytes of data memory (RAM), input/output lines, and a serial port. The microcomputer is clocked by an external 9.126-MHz clock generator. (This generator also provides 1152-kHz and 576-kHz signals for the actuator servo control demodulator and a 360-Hz signal for the spindle motor speed control circuit.)

The programmed logic array is a custom-designed IC which augments the operation of the microprocessor. Functions handled by the PLA include status logic, write fault monitor, read/write selection, and step control.

3-54. MICROPROCESSOR/PLA CONTROL SIGNALS

Signals generated by the microprocessor for control purposes within disc drive assembly A1 include: Seek, Odd In, Pick, Counter Reset, Normal Regulation, Stop Motor, Inner Track, Servo Enable, Even In, Velocity Command, Speed, and Seek Complete. PLA-generated signals include Write Gate, Seek Complete, Write Fault, and Ready.

Signals input to the microprocessor from circuitry internal to disc drive assembly A1 include: Power On Reset, Index, At Speed, Count Not Ready, Fault, Track 0, Off Track, On Peak, Direction In, Write Gate, and 9.216-MHz clock. Internal inputs to the PLA include Power On Reset, Fault, Write Gate, Drive Select, Stop, Seek Complete, and At Speed.

3-55. CLOCK GENERATOR

The clock generator consists of a crystal oscillator and a number of count-down registers. The clock generator has five outputs -- 9.216 MHz for the microprocessor, 1152 kHz and 576 kHz for the demodulator in the actuator servo control circuit, 92.1 kHz for the spindle speed checker circuit, and 360 Hz for the spindle speed control circuit.

3-56. HEAD-DISC MODULE

Details of the components contained in the sealed head-disc module are provided in the following paragraphs. See sheet 1C .

3-57. ACTUATOR. The read/write heads and servo head are mounted on a rotary arm supported by precision ball bearings. A bobbin-type voice coil, attached to the rotary arm, and mounted between two permanent magnets comprise a rotary voice-coil head positioning mechanism (actuator). This mechanism provides the driving force required to move the rotary arm for head positioning. The magnetic field in the gap between the magnets allows the acceleration of the rotary arm to be controlled by the voice-coil current. Drive current for the voice coil is supplied by the actuator servo control circuit. Crash stops are provided to protect the heads should a malfunction cause the actuator servo control circuit to lose control. When the disc drive is powered down, the rotary arm is driven to a nondata head landing zone at the inner diameter of the discs. Simultaneously, the arm is automatically locked over the landing zone to prevent possible head/medium damage if the disc drive is inadvertently subjected to excessive shock during relocation or shipment. Drive current for the actuator lock solenoid is supplied by an actuator lock driver circuit.

3-58. RECORDING MEDIUM. The recording medium is a plated metal magnetic coating on either side of a 130-millimetre (5.12-inch) diameter aluminum substrate. In the HP 7941, there are two such discs in the sealed head-disc module, with three surfaces used for data and one surface used for prerecorded servo information. The servo information is recorded on the lower surface of the bottom disc in the stack. In the HP 7945, there are four discs, with seven surfaces for data and one surface for servo information. Again, the servo information is recorded on the lower surface of the bottom disc in the stack.

3-59. READ/WRITE HEADS. The disc drive employs Winchester technology read/write heads, one for each data surface. The heads are designed to fly above the discs supported by a thin cushion of air which acts as an air bearing to the heads.

The flying height is approximately 16 microinches at the inner diameter of the disc. When the disc drive is powered down, the actuator moves the heads to the landing zone at the inner diameter of the discs where the heads come to rest on the surface.

Each head consists of a gapped ferrite core mounted in a ceramic slider. There are two windings wound around the ferrite core and the windings are connected at a common point and phased such that the common point acts as a center tap. These windings are used for both reading and writing by detecting or producing a magnetic field at the gap in the ferrite core.

In a write operation, data is written by passing a current through the windings of the selected head. This current generates a flux field across the gap and aligns the magnetic particles contained in the coating on the surface of the disc. The writing process orients the poles of each magnetized particle to store the direction of the flux field as the particles pass beneath the head. The direction of the flux field is a function of the write current direction. Erasing is accomplished by writing over any data which may have been previously recorded on the disc.

In a read operation, as the data surface passes beneath a head, the magnetically stored flux fields intersect the gap in the ferrite core. Gap motion through the flux field causes a voltage to be induced into the windings wound around the core. This induced voltage is analyzed by the read circuitry to define the data recorded on the surface of the disc. Each flux reversal, caused by a write current polarity change, generates a readback voltage pulse.

There are read preamplifier/write driver IC's mounted on the rotary arm of the actuator, adjacent to the heads. Each IC provides write current, head selection, and read signal amplification for four read/write heads. The IC's are connected to the read/write data channel electronics external to the sealed head-disc module via a flexible printed-circuit cable.

3-60. READ PREAMPLIFIER/WRITE DRIVER IC. The read preamplifier/write driver IC is standard integrated circuit designed for disc drive read/write head control. The IC can select 1 of 4 heads, read from or write to the selected head, and supply a write fault signal. One IC is used in the HP 7941. There are two IC's in the HP 7945. Control signals for the IC's are supplied by the head select and control logic block.

The IC is enabled by Chip Enable signal CE-L. Binary Head Select signals HS1-H, HS2-H are decoded by the IC to select the desired head. Reading and writing is controlled by Write Select signal WS. When WS is high, the write mode is selected, and when WS is low, the read mode is selected.

When the IC is in write mode, differential current applied across the DX, DY lines is used to switch the current drawn from the write current source to the head of the selected channel. Head voltage swings, generated by the switching of write current through the inductive head, are monitored by a head transition detect circuit in the IC. Absence of proper head voltage swings indicates an open or short in either half of the head winding, or an absence of write current. The absence of voltage swings will cause a current to flow into the Unsafe (US) output line. This line is connected to the fault detector, which will pass a write fault message to the PLA.

When the IC is in read mode, data is read from the selected head, amplified, and output on the differential DX, DY lines to the read chain amplifier and signal conditioner. If a fault condition exists such that write current is applied to the IC when it is in the read mode, the write current will be drawn from the Unsafe line and the fault will be detected by the fault detector.

3-61. SERVO HEAD. The servo head is a read only head constructed similarly to the read/write heads. The output of the head is amplified by a servo preamplifier IC mounted on the rotary arm of the actuator.

3-62. SERVO PREAMPLIFIER IC. The servo preamplifier IC is a 2-stage differential amplifier designed for use as a preamplifier for a magnetic servo head. The preamplifier output, labeled SERVO+, SERVO-, is connected to the input of the actuator servo control demodulator via the flexible printed-circuit cable used to connect the read preamplifier/write driver IC signal lines to the read/write data channel.

3-63. SPINDLE MOTOR. The spindle motor is a 3-phase brushless dc motor which spins the discs at a speed of 3,600 rpm. Incorporated in the motor are three Hall-effect sensors which are used by the spindle speed control circuit to indicate which of the three phases should be driven. A fourth Hall-effect sensor in the motor provides a start of track Index signal. Signal Index is used for timing purposes within A1 and is passed via an output buffer to the ST-506 Interface as Index signal INDX-L.

3-64. AIR FILTRATION COMPONENTS. A self-contained recirculating filter supplies clean air through a 0.3 micron filter to the sealed head-disc module. A separate filter allows for ambient pressure equalization within the sealed head-disc module without the introduction of contaminants.

3-65. ACTUATOR LOCK DRIVER

The actuator lock is controlled by a solenoid which is energized at power-on after the microprocessor detects that the spindle motor is up to speed (At Speed signal true). At this time, the microprocessor activates its Pick line which in turn causes the actuator lock driver to energize the lock solenoid. The actuator arm is now released, allowing the heads to move over the discs.

3-66. SPINDLE SPEED CONTROL

The three Hall-effect sensor outputs from the spindle motor are input to a ROM commutator in a solid-state spindle speed control circuit which decides which of the three outputs from the circuit should be driven to spin the motor in the proper direction. The speed of the motor is controlled by a phase-locked frequency regulator which compares a 360-Hz signal from the clock generator with the signals from the three Hall-effect sensors. This regulator circuit provides feedback to drivers in the speed control circuit such that the speed of the motor is maintained at 3,600 rpm, plus or minus 3.6 rpm.

At power-on, after the Power On Reset signal is turned off, the microprocessor sets the Stop Motor signal false, causing the spindle motor dynamic brake to activate. At the same time, the microprocessor disables the spindle speed control circuit by deactivating the Normal Regulation line. This allows the spindle motor to accelerate without any speed regulation. The microprocessor monitors the motor speed by measuring the time interval between the Index pulses from the spindle motor. When the time interval between the pulses indicates that the speed is within one percent of 3,600 rpm, the microprocessor enables the speed control circuit by activating the Normal Regulation line. The microprocessor stops the spindle motor by application of the Stop Motor signal to the spindle speed control and relay driver circuits.

3-67. SPINDLE SPEED CHECKER

The spindle speed checker circuit monitors the speed of the spindle motor by comparing the frequency of the Index pulses from the spindle motor hall-effect sensor with a 92.1-kHz clock signal from the clock generator. The microprocessor monitors the At Speed and Counter Not Ready outputs from the speed checker circuit and shuts down operation of the disc drive if the speed is determined to be outside of a predetermined range.

3-68. SPINDLE MOTOR BRAKE RELAY AND RELAY DRIVER

The spindle speed control circuit includes a dynamic brake which brings the spindle motor to a rapid halt when the microprocessor issues a Stop Motor signal. Signal Stop Motor activates the relay driver which in turn causes the spindle motor brake relay to connect low-value resistors across the winding of the spindle motor. At the same time, signal Stop Motor, input to the speed control circuit, disables the 3-phase drive to the motor.

3-69. ACTUATOR SERVO CONTROL

Actuator positioning and head track following is achieved on a closed-loop basis using a dedicated servo surface. The servo information is written on the bottom surface of the bottom disc. The servo system employs a dual-frequency technique based on an amplitude difference between alternating servo tracks written at two different frequencies. On track is realized for a data head when the servo head is positioned exactly between two servo tracks. In operation, a demodulator circuit continuously samples the two frequencies from the servo head, sums and averages the two signals, and produces a position error signal (PES). This PES signal is linearly proportional to the error (off track) amount and also indicates the off track direction.

During track following, the PES voltage is input to a transconductance power amplifier which supplies drive current to the actuator voice coil. This causes the actuator to hold the servo head at a point where the PES voltage is zero -- exactly between the two servo tracks. Since the servo head and the read/write heads are fixed on the rigid rotary arm of the actuator, any movement of the servo head is translated to all of the read/write heads.

Signal PES is also used during a seek operation. As the rotary arm is moving across the discs during a seek, the PES voltage is a series of positive and negative peaks which the microprocessor counts to determine track location. Also, the slope of the PES voltage is used to determine the velocity of the rotary arm during the seek operation.

The dual-frequency technique described above is relatively insensitive to servo surface medium defects. Also, servo head azimuth alignment is not a critical factor in the operation of the system.

The actuator servo control circuitry includes a demodulator, mode select switch, tachometer, digital-to-analog converter (DAC), and amplifier. Details of these circuits are provided in the following paragraphs.

3-70. DEMODULATOR. The Servo+, Servo- signal (read from the servo surface via the servo head and the servo preamplifier IC) consists of a combination of the frequencies recorded on alternate servo tracks -- 700 kHz and 1020 kHz. This signal is amplified and then separated into two frequencies by two identical mixer channels in the demodulator. In one channel, the 700 kHz is mixed with 576 kHz from the clock generator to produce 124 kHz. In the other channel, the 1020 kHz is mixed with 1152 kHz from the clock generator to produce 132 kHz. Higher frequencies are attenuated with active low-pass filters in the mixer channels. The two outputs from the mixer channels are rectified, averaged, and fed to the input of a difference amplifier. The output of this amplifier is Position Error Signal PES. When the servo head is positioned exactly between two servo tracks (read/write head on track), PES is zero. Displacement from this position (read/write head off track) cause PES to go either positive or negative, depending on the direction of offset and with an amplitude equal to the amount of the offset. A PES level of 1 volt equals a displacement of approximately 100 microinches.

The rectified and averaged outputs from the two mixer channels are also fed to a summing and AGC amplifier which supplies an AGC voltage to the amplifier at the input of the demodulator.

The demodulator also contains a track zero detector. This circuit senses the presence of a third frequency (1100 kHz) recorded on the servo surface to identify track zero. The Track 0 output from the detector is coupled to the microprocessor which in turn transmits Track Zero signal TRK0-L on the ST-506 Interface.

3-71. MODE SELECT SWITCH. The mode select switch is a solid-state circuit which places the actuator servo control circuitry in either a seek (velocity) or track follow mode of operation. Operation of the switch is controlled by the Seek signal from the microprocessor.

3-72. SEEK MODE. The seek mode of operation is selected by the microprocessor when it switches the mode select switch to the seek position with its Seek line. This selects a number of circuit blocks which together comprise a negative feedback servo control system supplying drive current to the actuator voice coil. These circuits include a velocity digital-to-analog converter (DAC), tachometer, slope selector, current inverter, on-peak detector, inverter, and power amplifier.

3-73. Velocity DAC. The velocity DAC is a standard integrated-circuit digital-to-analog converter which outputs a velocity error dc voltage to the servo system in response to an 8-bit velocity error command from the microprocessor.

3-74. Tachometer. The tachometer provides a measurement of the actuator velocity by integrating the slope of the PES signal as the actuator crosses tracks. However, the PES voltage becomes non-linear at the peaks of its triangle-shaped waveform. Therefore, at this time the power amplifier current to the actuator voice coil is differentiated to provide an indication of actuator velocity.

3-75. Slope Selector. The slope selector circuit, programmed by the Even In signal from the microprocessor, selects a PES slope of the proper polarity for the tachometer to provide a negative feedback.

3-76. Current Inverter. The current inverter, with a gain of plus or minus one and programmed with the Odd In signal from the microprocessor, selects a current of the proper polarity from the power amplifier for input to the tachometer.

3-77. On-Peak Detector. The on-peak detector operates at approximately 3.5 volts to initiate the switch between the integrated PES signal and the differentiated motor current in the tachometer. The output of the on-peak detector is also coupled to the microprocessor to signal track crossings.

3-78. Power Amplifier. The power amplifier is a transconductance amplifier which supplies current to the actuator voice coil in response to an error voltage input. The amplifier output lines are labeled VCMA, VCMB. The amplifier is enabled by the Servo Enable line from the microprocessor.

3-79. Inverter. The inverter has a gain of plus or minus one and is programmed with signal Odd In from the microprocessor. The purpose of the inverter is to select an error voltage of the correct polarity for input to the power amplifier. The input to the inverter is from the tachometer (seek mode) or signal PES (track follow mode), as selected by the mode select switch.

3-80. TRACK-FOLLOW MODE. The track-follow mode of operation is selected by the microprocessor at the end of a seek operation when the addressed track has been reached. Signal PES is applied via the track-follow position of the mode select switch through the inverter to the input of the power amplifier. Signal Odd In from the microprocessor programs the inverter to select a PES voltage of the proper polarity to provide a negative feedback signal to the amplifier.

3-81. OFF-TRACK DETECTOR. The off-track detector monitors the amplitude of the PES signal and provides an Off Track output to the microprocessor whenever the PES voltage exceeds plus or minus 1.5 volts.

3-82. SEEK OPERATION. The disc drive must have Ready RDY-L and Seek Complete SKCMP-L true before a seek operation can begin. With the disc drive in this state, the microprocessor is in its basic loop, monitoring Motor Speed, Off Track, and looking for either a Step STEP-L pulse or Write Gate WGATE-L, both of which are gated by Drive Select DS0-L. When a Step pulse is received, the Step signal forces Seek Complete SKCMP-L false. If Write Gate is true and Seek Complete goes false, a fault condition will be issued, automatically deactivating the write circuitry. When a Step pulse is received and Write Gate in not true, then the microprocessor will initiate a seek operation. The microprocessor will set the direction of the seek from the information on the Direction DIR-L line. The microprocessor will also set the seek mode, at which time the actuator servo control circuit will cause the actuator to move. The speed at which the actuator moves is dependent on the rate at which the Step pulses are received. Maximum performance of the actuator is attained if the time interval between Step pulses is less than 39 microseconds.

The microprocessor counts the track crossings until there are no more Step pulses and the actuator is crossing the last track. At this time, the microprocessor switches the actuator servo control from the seek mode to the track follow mode. The microprocessor now starts a settling timer and looks for an off-track condition. If an off-track condition exists, the microprocessor restarts the settling timer. This is done until the off-track condition is cleared plus the settling time. Once this is accomplished, the microprocessor sets Seek Complete line SKCMP-L.

3-83. RESTORE TO TRACK 0 OPERATION. To perform a restore to track 0 operation, the microprocessor enables the actuator servo control circuit and moves the actuator over the data area and out of the landing zone into the outer guard band area. Once the microprocessor detects that the actuator is in the outer guard band area, the microprocessor will cause the actuator servo control circuit to settle the actuator on a data track. The microprocessor will set direction out with a slow velocity, and count the track crossings until the track zero signal is detected. The microprocessor will now cause the servo control circuit to lock onto a track and check for the track 0 signal. After the servo control circuit is locked onto track

0, the microprocessor will initiate its maximum and minimum track counter. When this is accomplished, the microprocessor will activate Drive Ready signal RDY-L and Seek Complete signal SKCMP-L.

3-84. READ/WRITE DATA CHANNEL

The read/write data channel includes head select and control logic, a read chain which amplifies and qualifies the differential MFM-encoded read signal from the read preamplifier/write driver IC's in the sealed head-disc module, and a write channel which converts the TTL-level MFM-encoded write data signal from SBC PCA-A5 into write current drive for the read preamplifier/write driver IC's.

3-85. HEAD SELECT AND CONTROL LOGIC

The head select and control logic block performs a hardware decode of ST-506 Head Select signals HS0-L through HS4-L and the Write Gate signal from the PLA. (Head Select line HS8-L is not used in the HP 7941 and HP 7945.) The output signals from the block enable the write driver/read preamplifier IC, select one of four read/write heads, and activate the read function or write function. The output lines are labeled Chip Enable CE0-L, CE1-L; binary Head Select bits HS1-H, HS2-H; and Write Enable WS. In the HP 7945, where two IC's are used to control seven heads, Chip Enable CE0-L selects one IC for controlling heads 0 through 3, and CE1-L selects the other IC for controlling heads 4 through 6. Signals HS1-L, HS2-H, and WS are input to both IC's.

3-86. READ CHAIN. The read chain receives differential current DX, DY from the read preamplifier portion of the read preamplifier/write driver IC's. This signal represents magnetic transitions seen by the head as it flies over the magnetic recording medium. Whenever the head passes over a magnetic transition, the preamplifier differential output peaks. The read chain amplifies this differential analog signal and converts it to a stream of differential logic-level pulses, one for every signal peak. These MFM-encoded pulses are sent to the DDC for decoding. The read chain circuitry includes an amplifier/signal conditioner stage and a differential line driver.

3-87. Amplifier/Signal Conditioner. In the amplifier section of the block, the differential DX, DY input is amplified, filtered and subjected to automatic gain control (AGC). A diode matrix at the input of the amplifier, controlled by the Write Enable signal from the microprocessor, isolates the read chain from the write chain during a write operation. The AGC circuit compensates for signal variations caused by normal differences in head flying height, head characteristics, and recording medium. The AGC circuit includes an AGC hold feature which maintains AGC control when switching between heads. Following AGC, the signal is filtered, differentiated, and input to a zero-crossing detector which converts the differential analog signals into logic-level pulses.

Circuitry in the signal conditioner portion of the block prevents noise in the analog input signal from producing false zero crossings. This is achieved by applying the output of the zero-crossing detector to a gating circuit which effectively screens out spurious pulses caused by noise.

3-88. Differential Line Driver. The conditioned output signal is coupled via a differential line driver to the ST-506 Interface. The output lines from the line driver are labeled RMFM+, RMFM-.

3-89. WRITE CHAIN. The write chain receives differential MFM-encoded write data from the device dependent circuits and converts the data to a differential signal suitable for transmission to the write driver section of the read preamplifier/write driver IC's. The write chain circuitry includes a line receiver, a transition generator, a write current source, and a write fault detector.

3-90. Line Receiver. The line receiver translates the differential MFM-encoded write data on the ST-506 Interface WMFM+, WMFM- lines into a single-ended format suitable for input to the transition generator. The output of the line receiver is a positive-going pulse for every magnetic transition to be written on the disc.

3-91. Transition Generator. The transition generator divides the MFM frequency by two so that the logic level of the output determines the direction of current through the head. Each transition in MFM generates a transition on the recording medium.

3-92. Write Current Source. The write current source provides current for the read/write heads and supplies a write control (WC) signal to the read preamplifier/write driver IC's. The write current source is enabled by the Write Gate line from the microprocessor and has two outputs, selected by the Inner Track line. For tracks 0 to 511, the write current output is 27.5 milliamperes and for tracks 512 and above, the write current is 22.5 milliamperes.

3-93. Write Fault Detector. During a write operation, the microprocessor monitors certain key parameters of the operation via the write fault detector. If an abnormal condition is detected, the microprocessor activates, via the PLA, Write Fault signal WFLT-L. Inputs to the write fault detector include Unsafe signal US from the write driver/read preamplifier IC, and lines from the write current source and the head select logic. The faults which can cause WFLT-L to become active are listed in table 3-1 under the description for signal WFLT-L.

3-94. SELF TEST

Disc drive assembly A1 performs a self-test of certain key hardware functions at power-on. These functions include head loading and seeking to track 0. Following successful completion of the tests, Ready RDY-L and Seek Complete SKCMP-L are set true, allowing A1 to respond to device dependent circuits commands via the ST-506 Interface. During normal operation of the disc drive, the microprocessor monitors spindle speed and off-track conditions. If either parameter exceeds predetermined limits, the microprocessor shuts down operation via the RDY-L and SKCMP-L lines.

3-95. POWER-ON RESET

The power-on reset circuit monitors the +5, +12, and -10 voltages in the disc drive. (The +5 and +12 voltages are input from power supply assembly A4 and the -10 volt supply is generated internally in disc drive assembly A1.) At power on, the Power On Reset output signal is active, holding the electronics in disc drive assembly A1 in a reset condition until the voltages reach their proper levels. During operation of the disc drive, if any one of the voltages falls below a predetermined level, Power On Reset will become active and shut down operation of the disc drive.

3-96. POWER SUPPLY A4

Power supply assembly A4 develops dc operating voltages from the ac line voltage and distributes these voltages throughout the disc drive. The power supply assembly also generates a power-on reset signal.

Power supply assembly A4 is a self-contained switch-mode power supply mounted on a printed-circuit assembly. See sheet 1A . Located in the assembly are all of the ac line voltage components including the line cord connector, line fuse, line voltage selector switch, line on/off switch, and line filter. Output voltages are +5 Vdc, +12 Vdc, and -12 Vdc. (The -12 Vdc output is not used in the HP 7941 and HP 7945 Disc Drives.) The power supply output voltages and power-on reset signal can be measured at test points at the front of PCA-A4. See figure 4-7. The output voltages are not adjustable. The power supply voltages are connected to single board controller PCA-A5 and disc drive assembly A1 via cable assembly W1.

The following paragraphs provide a more detailed description of the power supply A4 circuitry, as shown in sheet 1A . Refer to table 3-1 for a description of the mnemonics used in sheet 1A and to figure 4-9 for detailed voltage and signal distribution information.

3-97. AC INPUT CIRCUITS

The ac line voltage is connected to power supply assembly A4 through a printed-circuit assembly (PCA) mounted ~AC LINE connector. A PCA-mounted ac line on/off switch controls both sides of the ac line into the power supply. The switch is operated by a LINE~ pushbutton projecting through an opening on the front panel of the disc drive. There is a fuse in the line side of the ac input following the power switch. The fuse value is the same (3A, 250V) for both 115-Vac and 230-Vac inputs. A line filter following the fuse reduces the level of line transients entering the power supply and the amount of switching noise leaving the power supply.

Also associated with the input circuitry is a VOLTAGE SELECTOR switch which selects line voltages of 115 Vac or 230 Vac. When the switch is in the 115 Vac position, a surge voltage

protection device protects the power supply from damage if it is inadvertently connected to 230 Vac.

3-98. SWITCH-MODE SUPPLY

The switch-mode supply consists basically of an ac-dc converter and a flyback-mode dc-dc converter. The ac-dc converter rectifies and filters the ac line voltage. This filtered dc operating voltage is supplied to the dc-dc converter. Included in the ac-dc converter are two thermistors that limit the initial power on surge current to approximately 25 amperes peak at 115 Vac and 230 Vac. The dc-dc converter chops the dc input into time-varying voltages, transforms them to lower levels and filters the outputs to supply the desired dc voltages of +5, +12, and -12 Vdc.

3-99. POWER-ON RESET

The power-on reset circuit is activated by the +5V output from power supply assembly A4 and produces Power Valid signal PVAL-H. At power on, PVAL-H remains low for at least 100 milliseconds after the +5V output reaches 4.75V or higher. Signal PVAL-H then goes to a high level. Signal PVAL-H will also go low for at least 500 microseconds prior to the +5V going below 4.75V. Signal PVAL-H can be monitored at a test point on the front of power supply PCA-A4. See figure 4-7. PVAL-H is connected to single board controller PCA-A5.

Table 3-1. List of Mnemonics

MNEMONIC	SIGNAL	SOURCE	DESCRIPTION
ATN-L	Attention	A5 1A	HP-IB management interface line used to specify how information on bidirectional Data I/O Bus DIO1-L through DIO8-L is to be interpreted and which device must respond to the information. When ATN-L is low , the DIO1-H through DIO8-H lines carry addresses or commands. When ATN-L is high, the DIO1-H through DIO8-H lines carry data.
CE0-L, CE1-L	Chip Enable, Bits 0,1	A1 1C	Enable the read preamplifier/write driver IC in the head-disc module of disc drive assembly A1.
CSA0-H thru CSA5-H	Control/Status Address Bus, Bits 0 thru 5	A5 1A	Signals used to access the device dependent registers which comprise the Control/Status Data Bus CSB0-H through CSB7-H. Output to SBC PCA-A5 1B.
CSB0-H thru CSB7-H	Control/Status Data Bus, Bits 0 thru 7	A5 1A / 1B	Bidirectional 8-bit bus used to pass control and status data between the host dependent circuits and device dependent circuits. Output to SBC PCA-A5 1B.
CSRS-L	Control/Status Read Strobe	A5 1A	Signal used to pass bytes from the device dependent circuits to the host dependent circuits over Control/Status Data Bus CSB0-H through CSB7-H. The bytes are of a status nature since recording medium information is passed over Read/Write Data Bus DATA0-H through DATA7-H. The read strobe generates a 500-nanosecond control/status bus read cycle. Output to SBC PCA-A5 1B.
CSWS-L	Control/Status Write Strobe	A5 1A	Signal used to pass control bytes from the host dependent circuits to the device dependent circuits over Control/Status Data Bus CSB0-H through CSB7-H. Output to SBC PCA-A5 1B.

Table 3-1. List of Mnemonics (Continued)

MNEMONIC	SIGNAL	SOURCE	DESCRIPTION
DATA0-H thru DATA7-H	Read/Write Data Bus, Bits 0 thru 7	A5 1A / 1B	Bidirectional 8-bit bus used to pass read/write data between the host dependent circuits and device dependent circuits or vice versa. See 1A and 1B.
DAV-L	Data Valid	A5 1A	HP-IB handshake line used to indicate availability and validity of information on Data I/O Bus DIO1-L through DIO8-L. DAV-L indicates to a receiving device that data is available.
DIO1-L thru DIO8-L	HP-IB Data I/O Bus, Bits 1 thru 8	A5 1A	HP-IB bidirectional data input/output (I/O) bus used for the transfer of data, commands, and other messages between the host computer and the SBC. Transfer is bit parallel, byte serial.
DIR-L	Direction	A5 1B	ST-506 Interface control signal. DIR-L defines the direction of motion of the read/write heads when Step signal STEP-L is pulsed. An inactive (high) DIR-L defines an "out" direction and when STEP-L is pulsed, the read/write heads move away from the center of the disc. Conversely, an active (low) DIR-L defines an "in" direction and the read/write heads move towards the center of the disc. Output to disc drive assembly A1 1C via cable W3.
DRIN-L/ DROUT-L	Data Request In/ Data Request Out	A5 1B	Tri-state DMA request lines used to transfer bytes over Read/Write Data Bus DATA0-H through DATA7-H. The "out" direction is defined as being from the host dependent circuits to the device dependent circuits. A device dependent circuits are programmed via Control/Status Data Bus CSB0-H through CSB7-H to drive a given request line. Output to SBC PCA-A5 1A.

Table 3-1. List of Mnemonics (Continued)

MNEMONIC	SIGNAL	SOURCE	DESCRIPTION
DS0-L	Drive Select, bit 0	A5 1B	When active (low), connects the ST-506 Interface control lines to disc drive assembly A1 interface circuitry. Output to disc drive assembly A1 1C via cable W3.
DSIN-L/ DSOUT-L	Data Strobe In/ Data Strobe Out	A5 1A	SBC-generated strobe lines which accomplish the transferring of data between the the host dependent circuits and the device dependent circuits Read/Write Data Bus DATA0-H through DATA7-H.
DX, DY	Differential Data	A1 1C	Differential signal lines to/from read preamplifier/write driver IC's.
EOI-L	End Or Identify	A5 1A	HP-IB control signal used to indicate the end of multiple byte transfers or used with signal ATN-L to perform a parallel polling sequence.
GREEN-L	Green	A5 1B	Drive for green LED in front panel FAULT/ON LINE indicator. Output to the front panel via cable W4.
HS0-L, HS1-L, HS4-L, HS8-L	Head Select, Bits 0 thru 8	A5 1B	ST-506 Interface control signals. These lines provide a means of selecting each individual read/write head in a binary-coded fashion. When all four lines are inactive, head 0 is selected. Output to disc drive assembly A1 1C via cable W3.
HS1-H, HS2-H	Head Select, Bits 1, 2	A1 1C	Head select bits input to read preamp/write driver IC's from the head select and control logic.
IFC-L	Interface Clear	A5 1A	HP-IB general management line used to place the interface system in a known quiescent state.
INDX-L	Index	A1 1C	ST-506 Interface control line. INDX-L is provided by disc drive assembly A1 once each revolution of the disc (16.67 milliseconds nominal) to indicate the beginning of a track.

Table 3-1. List of Mnemonics (Continued)

MNEMONIC	SIGNAL	SOURCE	DESCRIPTION
			Normally, the signal is a high level and the transition to a low level indicates the start of a track. The signal is generated by a Hall-effect sensor in the spindle motor. Output to SBC PCA-A5 1B via cable W3.
NDAC-L	Not Data Accepted	A5 1A	HP-IB handshake line used to indicate the acceptance of data by all devices.
NRFD-L	Not Ready For Data	A5 1A	HP-IB handshake line used to indicate that all devices are, or are not, ready to accept data over Data I/O Bus DIO1-H through DIO8-H.
PES	Position Error Signal	A1 1C	Actuator servo control circuit signal indicating amount and direction of head off-track displacement.
PVAL-H	Power Valid	A4 1A	Indicates that power supply A4 outputs are up to their proper values. Output to SBC PCA-A5 1B via cable W1.
RDY-L	Ready	A1 1C	ST-506 Interface control signal. RDY-L becomes active (low) following power on if a) dc voltages are within specification, b) discs are at speed, and c) head position is recalibrated. Output to SBC PCA-A5 1B via cable W3. If there is a fault in the dc voltages or spindle speed control, RDY-L will remain inactive (high). RDY-L will not go low until the fault is cleared and the head position is recalibrated. After power on, RDY-L should become active within 25 seconds. During operation of the disc drive, the processor is continually monitoring the speed of the spindle motor. If a speed variation of greater than 2 percent is detected, the processor will force RDY-L high, lock the actuator, and stop the motor. Power on recycling is required to restart the disc drive.

Table 3-1. List of Mnemonics (Continued)

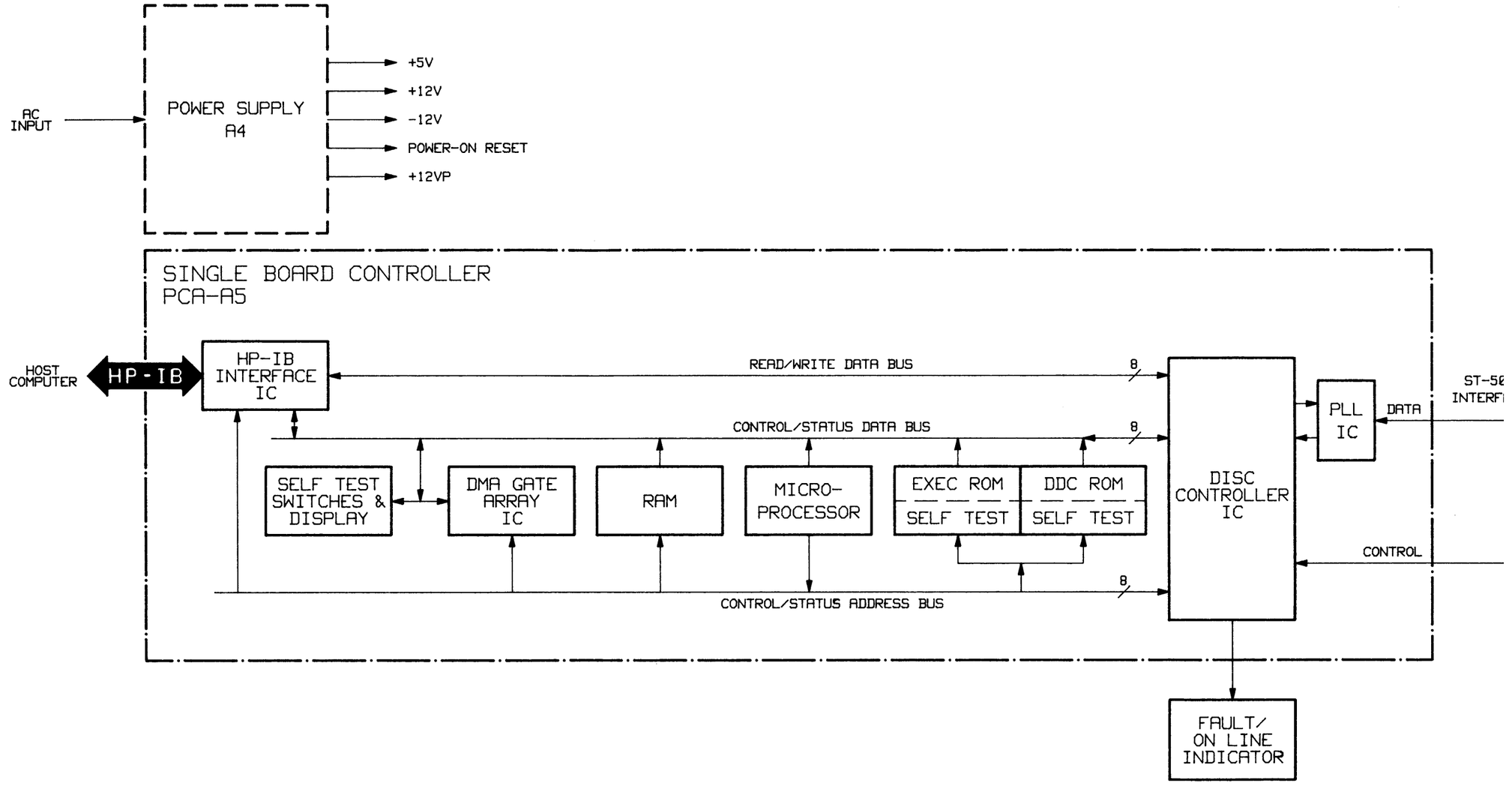
MNEMONIC	SIGNAL	SOURCE	DESCRIPTION
RED-L	Red	A5 1B	Drive for red LED in front panel FAULT/ON LINE indicator. Output to the front panel via cable W4.
REN-L	Remote Enable	A5 1A	HP-IB control line used in conjunction with other messages to select between two alternate sources of device programming data.
RMFM+, RMFM-	MFM Read Data	A1 1C	ST-506 Interface data signal. A differential signal which defines the MFM transitions recovered by reading a prerecorded track with a selected head. The transition of the RMFM+ line going more positive than the RMFM-line represents a flux reversal on the track. Output to SBC PCA-A5 1B via cable W4.
SEL-L	Select	A5 1A	DC-IB signal used to select which DDC will respond to a given control/status bus operation. When low, SEL-L selects DDC (disc drive.)
SKCMP-L	Seek Complete	A1 1C	ST-506 Interface control signal. SKCMP-L indicates that the read/write heads have settled on the final track at the end of a seek operation. Reading or writing should not be attempted when SKCMP-L is inactive (high). Output to SBC PCA-A5 1B via cable W3.
SRQ-L	Service Request	A5 1A	HP-IB general management line. SRQ-L is used by a device to indicate the need for service and to request an interrupt of the current activity.
STEP-L	Step	A5 1B	ST-506 Interface control signal. STEP-L causes the read/write heads to move in the direction of motion defined by Direction signal DIR-L. One Step pulse = one step = one track. Output to disc drive assembly A1 1C via cable W3.
TRK0-L	Track 0	A1 1C	Indicates when the read/write heads are positioned at cylinder 0 (the outermost data track). Output to SBC PCA-A5 1B via cable W3.

Table 3-1. List of Mnemonics (Continued)

MNEMONIC	SIGNAL	SOURCE	DESCRIPTION
US	Unsafe Current	A1 1C	A read preamplifier/write driver line in which current flows whenever writing is enabled and there is an absence of write current or data transitions.
VCMA, VCMB	Actuator Voice Coil Drive	1A 1C	Drive current to actuator voice coil. Signal is supplied by actuator servo control circuit.
WC	Write Current	1A 1C	A line from the write current source sending current to the read read/write head during a write. Output to the read preamplifier/ write driver IC's.
WFLT-L	Write Fault	A1 1C	ST-506 Interface control signal. WFLT-L warns that a condition exists in disc drive assembly A1 which makes writing unsafe. Output to SBC PCA-A5 1B via cable W2. Signal becomes active for the following reasons. WRITING: • Open head. • Shorted head. • Improper write current. • An offtrack condition occurs. • Invalid or multiple heads are selected. • Spindle speed loss when writing. • A write is attempted when SKCMP-L is inactive (high). • Write gate but no write data. • Attempting to write with RDY-L inactive (high). • A write attempted when the disc drive is write protected with the write protect option. READING: • Write current appears at head. Disc drive assembly A1 will not accept further commands after a write fault has been detected by the microprocessor.

Table 3-1. List of Mnemonics (Continued)

MNEMONIC	SIGNAL	SOURCE	DESCRIPTION
			If the disc drive is deselected, the microprocessor will reexamine the fault and reactivate itself if the condition clears.
WGATE-L	Write Gate	A5 1B	ST-506 Interface control signal. When WGATE-L is active (low), it enables write data to be written on the disc. When inactive (high), it enables data to be read from the disc. Output to disc drive assembly A1 1C via cable W3.
WMFM+, WMFM-	MFM Write Data	A5 1B	ST-506 Interface data signal. A differential MFM signal which defines the transitions to be written on a track. The transition of the WMFM+ line going more positive than the WMFM-line will cause a flux reversal on a track (provided that Write Gate WGATE-L is active). Output to disc drive assembly A1 1C via cable W2.
WS	Write Select	A1 1C	Selects the read or write mode of operation for the preamplifier/write driver IC's in the head-disc module. When WS is high, the write mode is selected; when WS is low, the read mode is selected.



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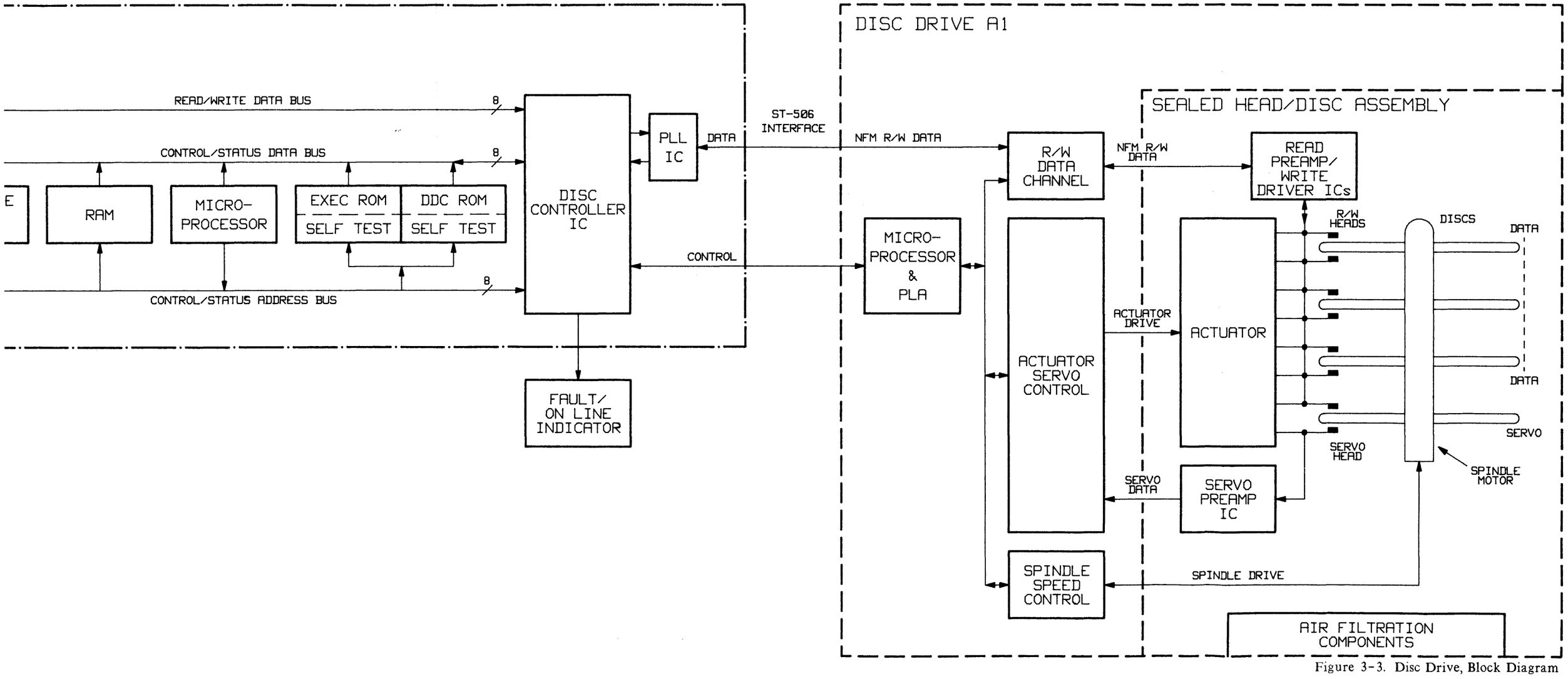
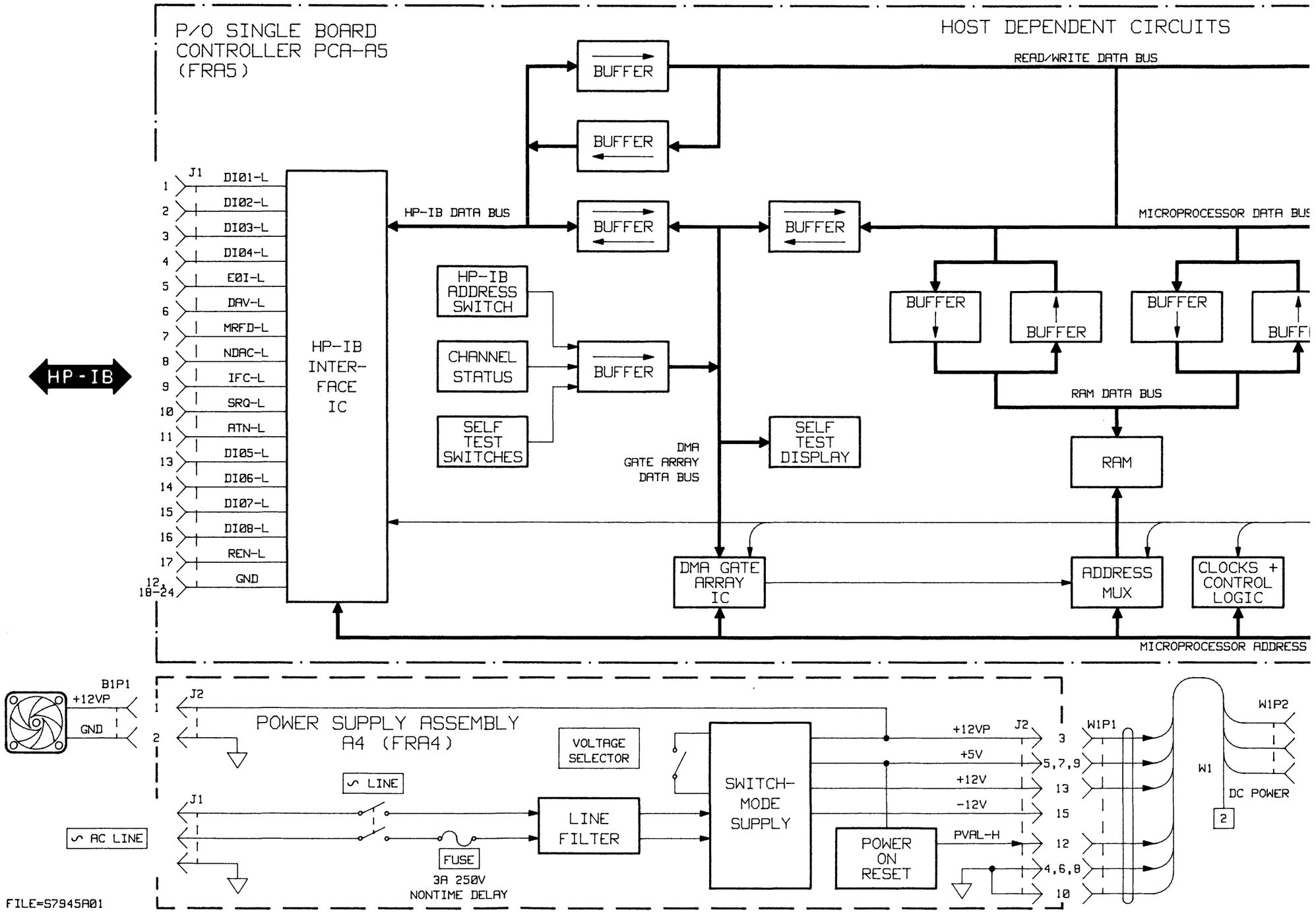


Figure 3-3. Disc Drive, Block Diagram


P/O SINGLE BOARD CONTROLLER PCA-A5 (FRA5)
HOST DEPENDENT CIRCUITS
HP-IB
J1
1
2
3
4
5
6
7
8
9
10
11
13
14
15
16
17
12, 18-24
DI01-L
DI02-L
DI03-L
DI04-L
EOI-L
DAV-L
MRFD-L
NDAC-L
IFC-L
SRQ-L
ATN-L
DI05-L
DI06-L
DI07-L
DI08-L
REN-L
GND
HP-IB INTER-FACE IC
HP-IB DATA BUS
BUFFER
HP-IB ADDRESS SWITCH
CHANNEL STATUS
SELF TEST SWITCHES
SELF TEST DISPLAY
DMA GATE ARRAY DATA BUS
READ/WRITE DATA BUS
MICROPROCESSOR DATA BUS
RAM DATA BUS
RAM
DMA GATE ARRAY IC
ADDRESS MUX
CLOCKS + CONTROL LOGIC
MICROPROCESSOR ADDRESS
B1P1
+12VP
GND
POWER SUPPLY ASSEMBLY A4 (FRA4)
VOLTAGE SELECTOR
LINE
AC LINE
FUSE
3A 250V NONTIME DELAY
LINE FILTER
SWITCH-MODE SUPPLY
POWER ON RESET
PVAL-H
+12VP
+5V
+12V
-12V
W1P1
W1P2
W1
DC POWER
FILE=S7945A01

HOST DEPENDENT CIRCUITS

READ/WRITE DATA BUS

READ/WRITE DATA BUS
DATA0-H - DATA7-H
8

DRIN-L
DSIN-L
DROUT-L
DSOUT-L

CONTROL/STATUS DATA BUS
CSB0-H - CSB8-H
8

CSRS-L
CSWS-L
PVAL-H

TO 1B

TA BUS

BUFFER

MICROPROCESSOR DATA BUS

HP-IB ADDRESS SWITCH

CHANNEL STATUS

SELF TEST SWITCHES

DMA GATE ARRAY DATA BUS

SELF TEST DISPLAY

RAM DATA BUS

RAM

MICRO PROCESSOR

EXEC ROM

DDC ROM

DMA GATE ARRAY IC

ADDRESS MUX

CLOCKS + CONTROL LOGIC

CONTROL/STATUS ADDRESS BUS
CSA0-H - CSA8-H
SEL-L

MICROPROCESSOR ADDRESS BUS

EMBLY

VOLTAGE SELECTOR

LINE FILTER

SWITCH-MODE SUPPLY

POWER ON RESET

+12VP
+5V
+12V
-12V
PVAL-H

J2
3
5,7,9
13
15
12
4,6,8
10

W1P1

W1

DC POWER

2

W1P2

J2
2 +5V
1 PVAL-L
5

50V DELAY

1A

Figure 3-4. Disc Drive, Functional Block Diagram, (Sheet 1 of 3)

P/O SINGLE BOARD CONTROLLER PCA-A5

DEVICE DEPENDENT CIRCUITS

FROM 1A

CSRS-L
CSWS-L
SEL-L
CSA0-H - CSA5-H
6
CONTROL/STATUS ADDRESS BUS

CONTROLLER IC & REGISTER DECODE LOGIC

CLOCK GEN
10 MHz
5 MHz

PHASE LOCKED LOOP IC

A0-A2

DISC CONTROLLER IC

SWITCH SW212

SELF-TEST REGISTER

GPC REGISTER

CSB0-H - CSB7-H
8
CONTROL/STATUS DATA BUS
STATUS

TRANS-CEIVER

LOOPBACK SELECT

DDC ERRORS REGISTER

PUPO REGISTER

RECEIVER

DRIVER

DATA0-H - DATA7-H
8
DISC READ/WRITE DATA BUS

DRIN-L
DSIN-L
DROUT-L
DSOUT-L

DMA HAND-SHAKE CONTROL

LATCH

ST-508 INTERFACE

W2
1C
DATA
W3P1 W2

RWFM+ J4 17
RRMFM- 18
WMFM+ 14
WMPN- 13
2,4,6,8,11,12, 10,15,16,19,20

W3
1C
CONTROL
W3P1 W3

SKCMP-L J3 8
TRK0-L 10
WFLT-L 12
INDX-L 20
RDY-L 22
STEP-L 24
DIR-L 34
WGATE-L 6

HSB-L 2
HS4-L 4
HS2-L 18
HS0-L 14
DS0-L 26
ALL ODD PINS. 1 THRU 33
GND

RED-L J5 3
GREEN-L 2
+5V 1
+5V 4

W4P1 W4 W4P2
3 RED
2
1 GREEN
4

FAULT/ON-LINE

+12V
+5V
PVAL-H
POWER ON RESET, ALL CIRCUITS.
J2
5 8 2 1,3

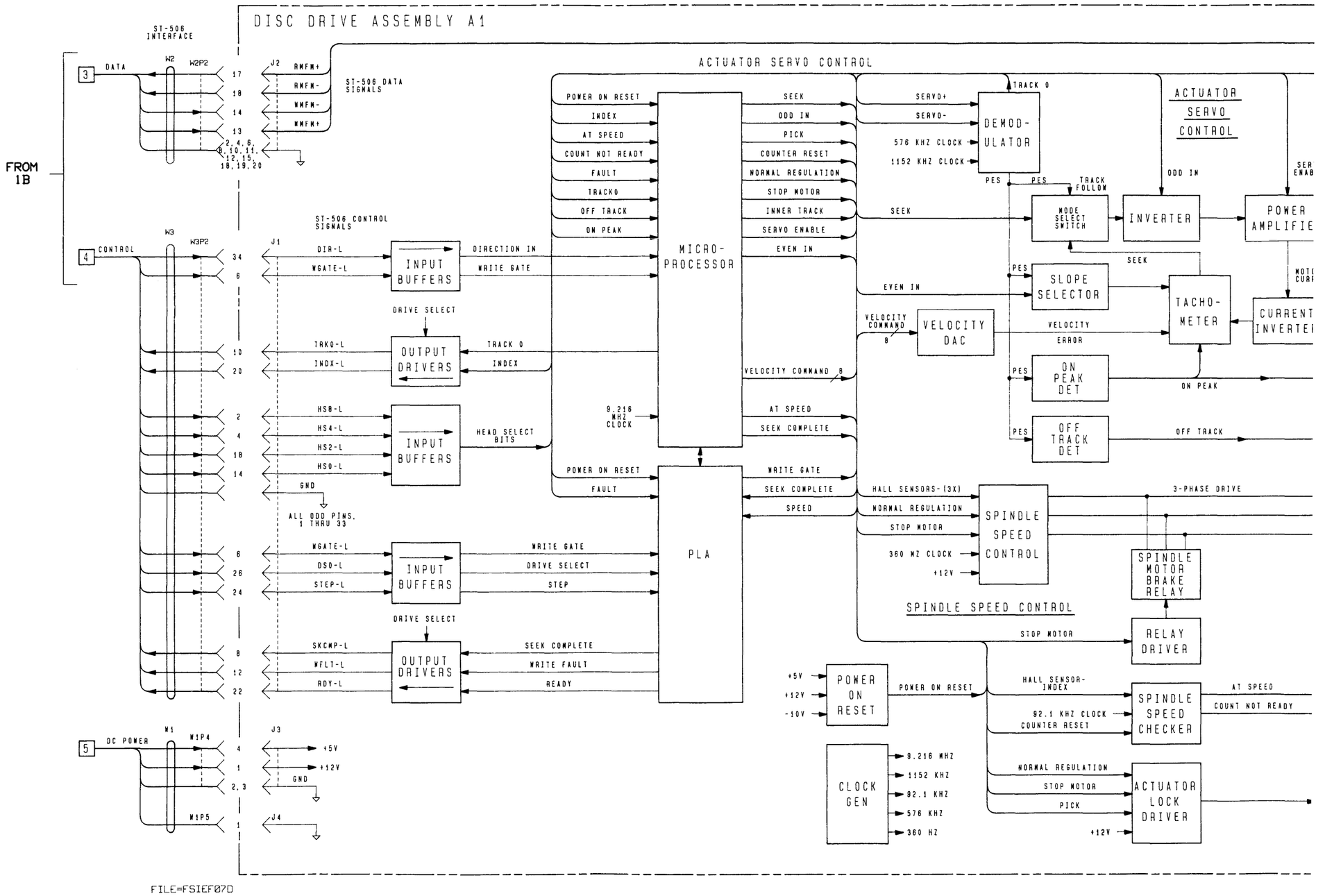
W1P2
W1

W1 DC POWER
2
DC POWER W1
5

1B

FILE=S7945A02

Figure 3-4. Disc Drive, Functional Block Diagram, (Sheet 2 of 3)


DISC DRIVE ASSEMBLY A1
ST-506 INTERFACE
ACTUATOR SERVO CONTROL
FROM 1B
3
DATA
W2
W2P2
J2
RWFM+
RWFM-
WWFM-
WWFM+
17
18
14
13
2, 4, 6, 8, 10, 11, 12, 15, 16, 19, 20
ST-506 DATA SIGNALS
4
CONTROL
W3
W3P2
J1
DIR-L
WGATE-L
34
6
ST-506 CONTROL SIGNALS
INPUT BUFFERS
DIRECTION IN
WRITE GATE
DRIVE SELECT
OUTPUT DRIVERS
TRK0-L
INDX-L
10
20
TRACK 0
INDEX
HS8-L
HS4-L
HS2-L
HS0-L
2
4
16
14
HEAD SELECT BITS
GND
ALL ODD PINS, 1 THRU 33
WGATE-L
DS0-L
STEP-L
6
26
24
WRITE GATE
DRIVE SELECT
STEP
SKCMP-L
WFLT-L
RDY-L
8
12
22
SEEK COMPLETE
WRITE FAULT
READY
5
DC POWER
W1
W1P4
W1P5
J3
J4
4
1
2, 3
1
+5V
+12V
GND
POWER ON RESET
INDEX
AT SPEED
COUNT NOT READY
FAULT
TRACK0
OFF TRACK
ON PEAK
MICRO-PROCESSOR
SEEK
ODD IN
PICK
COUNTER RESET
NORMAL REGULATION
STOP MOTOR
INNER TRACK
SERVO ENABLE
EVEN IN
VELOCITY COMMAND 8
9.216 MHZ CLOCK
AT SPEED
SEEK COMPLETE
WRITE GATE
SEEK COMPLETE
SPEED
PLA
SERVO+
SERVO-
576 KHZ CLOCK
1152 KHZ CLOCK
DEMOD-ULATOR
TRACK 0
PES
TRACK FOLLOW
MODE SELECT SWITCH
SEEK
INVERTER
ODD IN
ACTUATOR SERVO CONTROL
POWER AMPLIFIE
SLOPE SELECTOR
EVEN IN
VELOCITY COMMAND
8
VELOCITY DAC
VELOCITY ERROR
TACHO-METER
CURRENT INVERTE
ON PEAK DET
ON PEAK
OFF TRACK DET
OFF TRACK
HALL SENSORS-(3X)
NORMAL REGULATION
STOP MOTOR
360 MZ CLOCK
+12V
SPINDLE SPEED CONTROL
3-PHASE DRIVE
SPINDLE MOTOR BRAKE RELAY
SPINDLE SPEED CONTROL
STOP MOTOR
RELAY DRIVER
+5V
+12V
-10V
POWER ON RESET
HALL SENSOR-INDEX
92.1 KHZ CLOCK
COUNTER RESET
SPINDLE SPEED CHECKER
AT SPEED
COUNT NOT READY
CLOCK GEN
9.216 MHZ
1152 KHZ
92.1 KHZ
576 KHZ
360 HZ
NORMAL REGULATION
STOP MOTOR
PICK
+12V
ACTUATOR LOCK DRIVER
FILE=FS1EF07D

DRIVE ASSEMBLY A1

ACTUATOR SERVO CONTROL

RMFM+
RMFM-
WMFM-
WMFM+
ST-506 DATA SIGNALS

ST-506 CONTROL SIGNALS
DIR-L
WGATE-L
INPUT BUFFERS
DIRECTION IN
WRITE GATE

DRIVE SELECT
TRK0-L
INDX-L
OUTPUT DRIVERS
TRACK 0
INDEX

HS8-L
HS4-L
HS2-L
HS0-L
INPUT BUFFERS
HEAD SELECT BITS
GND
LL ODD PINS, 1 THRU 33

WGATE-L
DS0-L
STEP-L
INPUT BUFFERS
WRITE GATE
DRIVE SELECT
STEP

DRIVE SELECT
SKCMP-L
WFLT-L
RDY-L
OUTPUT DRIVERS
SEEK COMPLETE
WRITE FAULT
READY

+5V
+12V
GND

POWER ON RESET
INDEX
AT SPEED
COUNT NOT READY
FAULT
TRACK0
OFF TRACK
ON PEAK

MICRO-PROCESSOR

9.216 MHZ CLOCK

PLA

SEEK
ODD IN
PICK
COUNTER RESET
NORMAL REGULATION
STOP MOTOR
INNER TRACK
SERVO ENABLE
EVEN IN
VELOCITY COMMAND 8
AT SPEED
SEEK COMPLETE
WRITE GATE
SEEK COMPLETE
SPEED

SERVO+
SERVO-
576 KHZ CLOCK
1152 KHZ CLOCK
DEMOD-ULATOR
TRACK 0
PES
TRACK FOLLOW
MODE SELECT SWITCH
SEEK
INVERTER
ODD IN
SERVO ENABLE
POWER AMPLIFIER
VCMA
VCMB
MOTOR CURRENT
CURRENT INVERTER
ODD IN
SLOPE SELECTOR
EVEN IN
VELOCITY COMMAND 8
VELOCITY DAC
VELOCITY ERROR
TACHO-METER
ON PEAK DET
ON PEAK
OFF TRACK DET
OFF TRACK

ACTUATOR SERVO CONTROL

HALL SENSORS-(3X)
NORMAL REGULATION
STOP MOTOR
360 MZ CLOCK
+12V
SPINDLE SPEED CONTROL
3-PHASE DRIVE
SPINDLE MOTOR BRAKE RELAY

SPINDLE SPEED CONTROL

STOP MOTOR
RELAY DRIVER

+5V
+12V
-10V
POWER ON RESET
POWER ON RESET
HALL SENSOR-INDEX
92.1 KHZ CLOCK
COUNTER RESET
SPINDLE SPEED CHECKER
AT SPEED
COUNT NOT READY

CLOCK GEN
9.216 MHZ
1152 KHZ
92.1 KHZ
576 KHZ
360 HZ

NORMAL REGULATION
STOP MOTOR
PICK
+12V
ACTUATOR LOCK DRIVER

WRITE CHAIN
READ CHAIN
WRITE GATE
WMFM+
WMFM-
LINE RECEIVER
TRANSITION GEN
WRITE GATE
DX
DY
AMPLIFIER/ SIGNAL CONDITIONER
DIFF LINE DRIVER
RMFM+
RMFM-

READ/WRITE DATA CHANNEL

SEALED HEAD-DISC ASSEMBLY

WRITE GATE
INNER TRACK
POWER ON RESET
WRITE CURRENT SOURCE
DX
DY
WC
READ PREAMP/ WRITE DRIVER IC'S
FAULT
WRITE FAULT DETECTOR
US

HEAD SELECT BITS
HS0-L THRU HS3L
WRITE GATE
HEAD SELECT + CONTROL LOGIC
CE0-L, CE1-L, HS1-H, HS2-H, WS

ACTUATOR
VOICE COIL
VCMA
VCMB
R/W HEADS
DISC
SERVO HEAD
SERVO+
SERVO-
SERVO PREAMP IC
3-PHASE DRIVE
SPINDLE MOTOR
3-PHASE DRIVE
HALL-EFFECT SENSORS-(3X) AND INDEX
ACTUATOR LOCK SOLENOID
AIR FILTRATION COMPONENTS

1C

Figure 3-4. Disc Drive, Functional Block Diagram, (Sheet 3 of 3)

SERVICE INFORMATION

4-1. INTRODUCTION

WARNING

The disc drive does not contain operator serviceable parts. To prevent electrical shock, refer all service activities to service-trained personnel.

CAUTION

- The field replaceable assemblies (FRA's) in the disc drive are electrostatic sensitive devices. Take appropriate precautions when removing the FRA's from the disc drive. Use of an anti-static pad and wrist strap is required. (These components are contained in anti-static work station, part no. 9300-0749.) Immediately after removal, store the FRA's in anti-static, conductive plastic bags.

- The disc drive is delicate and should be handled with care. Also, the disc drive is heavier (9.9 kilograms/21.8 pounds) than its size would indicate.

- Do not turn the LINE~ switch on or off when the system is transferring data on the Hewlett-Packard Interface Bus (HP-IB).

- Do not cycle the LINE~ switch on and off unnecessarily.

- Do not connect or disconnect the HP-IB cable(s) from the disc drive when the system is transferring data on the HP-IB.

This section contains information useful for troubleshooting the disc drive. This information includes a description of the disc drive self-test and internal diagnostic routines, troubleshooting hints, and details of signal connections and power distribution.

4-2. SERVICE TOOLS

The following tools and materials are required to service the disc drive:

- Torx* T10 Driver
- Torx* T15 Driver
- Torx* T25 Driver
- Nut Driver, 9/32"
- Pozi Driver, No. 1
- Anti-Static Work Station, part no. 9300-0794

4-3. FRA LOCATIONS

The locations of the three field replaceable assemblies (FRA's) identified by the self-test diagnostics are shown in figure 4-3, Field Replaceable Assembly (FRA) Locations. Refer to section V for FRA removal and replacement instructions and to section VI for FRA identification and ordering information.

4-4. CABLE CONNECTORS

Figures 4-4 through 4-7 show the locations of the cable connectors on the three FRA's in the disc drive and the cables coupled to these connectors. Figure 6-1, Disc Drive, Exploded View, shows how the cables are connected between the FRA's. An overall cabling diagram of the disc drive is provided in figure 4-8, Cabling Diagram.

*TORX is a registered trademark of the Camcar Division of Textron, Inc.

4-5. SIGNAL DISTRIBUTION

Cable connections between the FRA's in the disc drive are shown in figure 4-8. The distribution of signals via these cables is shown in figure 4-9, Signal Distribution. The mnemonics appearing in figure 4-9 are defined in table 3-1, List of Mnemonics.

4-6. POWER DISTRIBUTION

Details of ac input wiring and dc power distribution are shown in figure 3-4, Disc Drive, Functional Block Diagram, Sheet 1, and in figure 4-8, Cabling Diagram.

4-7. SIGNAL NOTATION

In the disc drive logic circuits, a digital signal is applied to its destination in one of two states: active or inactive. The signal is active when its voltage level (high or low) makes the action occur for which the signal was designed. This action is usually identified by a signal mnemonic. Refer to table 3-1, List of Mnemonics. A mnemonic with an "-L" suffix indicates a logic signal with an active low voltage level. A mnemonic with an "-H" suffix indicates a logic signal with an active high voltage level. Signal mnemonics without an "-L" or "-H" suffix usually indicate analog, data bus, or control bus signals.

4-8. BLOCK DIAGRAM

A functional block diagram of the disc drive is provided in section III of this manual. (See figure 3-4.) To facilitate references to the three sheets of this diagram, each sheet is identified by a large bold numeral in the lower right-hand corner of the page. These numerals are boxed in text and table references, for example: **1A** . Included in figure 3-4 are diagrams for single board controller FRA5 **1A** , **1B** , disc drive assembly FRA1 **1C** , and power supply assembly FRA4 **1A** . Each of these diagrams in section III is accompanied by a circuit description.

4-9. TEST POINTS

A number of test points are provided in power supply FRA4 for troubleshooting and test purposes. The location of these test points is shown in figure 4-7, FRA4 (Power Supply A4), Test Points and Voltages. Also provided are specifications for the voltages monitored at the test points. The output voltages are not adjustable. It should be noted that access to the test points requires the removal of the front panel assembly from the disc drive. Refer to Section V for removal details.

4-10. SELF-TEST CONTROLS

The disc drive self-test controls include a red/green FAULT/ON LINE indicator on the front panel, together with two switches and a 2-digit hexadecimal Self-Test display on the rear panel. See figure 4-1, Self-Test Controls and Readout. Information regarding the use of these controls and indicators is provided in the following paragraphs.

4-11. FAULT/ON LINE INDICATOR

The FAULT/ON LINE indicator is a red/green display which signals the operating status of the disc drive. When line voltage is applied to the disc drive, the FAULT (red) and ON LINE (green) portions of the display will illuminate for one second to verify that the display is functioning. Next, the green portion will flash during the time that the disc drive is executing its internal self-test routines. Self test takes between six and twelve seconds to complete. If the disc drive passes self test, the display will change to a solid green. If the disc drive fails self test, the display will change to a solid red with a flashing green indicating that the self test failure has occurred, but that the self test routines are still accomplishing some "housekeeping" tasks. When these tasks are complete, the green indicator will extinguish, indicating that the disc drive is ready to accept host commands such as diagnostics. The green indicator will flash again when the disc drive attempts to respond to these commands. A solid red and green display indicates that the single board controller has failed self test.

After a successful self test, a solid green display indicates that the disc drive is idle and a flashing green display indicates that the disc drive is active.

4-12. SELF TEST SWITCH

The SELF TEST switch is a momentary contact pushbutton switch which initiates the disc drive internal self-test diagnostic routines. The switch is recessed behind the rear panel and can be activated by the tip of a ball point pen or similar object. The self-test routines initiated by the switch are the same as those initiated by a host-issued diagnostic command. Both of these routines are similar to the power on self-test routines except that certain host dependent controller (unit 2) subtests are not executed as these subtests would destroy the current runtime environment.

4-13. SELF-TEST DISPLAY

The Self-Test display consists of a 2-digit 7-segment hexadecimal display which reports the results of the internal self-test and diagnostic routines. Whenever self test is initiated, either by operation of the SELF TEST switch or when line voltage is applied, the display will first show a **8.8.** readout to indicate that all segments of the display are functioning. The display will then go blank until self test is completed. In the case of a self-test command issued by the system to unit 0, the display will immediately go blank (**8.8** is not displayed) and remain blank until self test is completed.

When the SELF TEST switch is pressed, release from the host is requested. If release is granted, the display is blanked to indicate that the self test is ready to start. When the switch is released, self-test commands are issued to the disc drive. One of the first tests is one that causes the **8.8.** display to appear. The display is then blanked until self test is completed. If release is not granted, a **r.d.** (release denied) display will appear. This message will continue to be displayed until the SELF TEST switch is released, at which time the display will show the previous pass/fail result.

When self test has been completed on the units of the disc drive (host dependent controller, disc drive, and power supply), the display will show a **P.X.** (pass) or a **F.X.** (fail) result. The numeral **X.** is the disc drive HP-IB device address.

Note: The decimal points in the display are tied directly to the host dependent controller +5 Vdc supply and signal the presence of this voltage. The decimal points should remain illuminated at all times during both self test and normal operation of the disc drive.

4-14. DISPLAY RESULTS SWITCH

The DISPLAY RESULTS switch is a momentary contact pushbutton switch which causes self test results to be displayed on the Self-Test display. The switch is operated in a similar manner to the SELF TEST switch. When the DISPLAY RESULTS switch is pressed, a request for release is generated. The switch must be pressed and held down until release is granted or denied. If release is granted the display will go blank until the switch is released. If release is denied when the switch is pressed, a **r.d.** message will be displayed. When the switch is released, the previous pass/fail result is restored to the display.

Note: In the event of a self-test failure, the disc drive will have requested release to update the error logs. If the disc drive is not operating correctly, this update operation may take some time to complete. During this period, the DISPLAY RESULTS switch will be inactive. This means that the DISPLAY RESULTS switch may have to be pressed for a longer than normal period of time or pressed after the update operation has been completed.

Following release, pressing the switch a number of times will display a sequence of test failure information. The information displayed for a failure will be, in order, unit failed, field replaceable assembly (FRA) failed, and subtest failed. The failing unit is indicated by the display **U.X.**, where numeral **X.** identifies the unit. The failing FRA is indicated by **A.X.**, where numeral **X.** identifies the FRA. A subtest failed is indicated by a 2-digit hexadecimal number. It is possible for a failing unit to have multiple failing FRA's. Multiple FRA's are listed in descending order of most probable failure. If a unit has no failures to report, it will display only the unit number. Refer to

figure 4-1 for a listing of unit and FRA numbers. Single board controller (unit 2) and disc drive (unit 0) subtest numbers, together with a brief description of the subtests, are listed in tables 4-1 and 4-2, respectively.

Note 1. The sequence mode described above is distinct from the pass/fail mode. When sequencing test results, *all* of the results must be displayed before the device will go back on-line (return from release). After the last result has been displayed, the display will return to **P.X.** (pass) or **F.X.** (fail).

Note 2. A unit 2 (single board controller) self-test failure is a special type of failure. When unit 2 fails self test, it will enter into an infinite loop monitoring the DISPLAY RESULTS switch. The only function that the disc drive can perform under this condition is to toggle out the unit 2 self-test results. The disc drive will not respond to any commands from the host computer. The red and green FAULT/ON LINE indicators will be illuminated at this time. Exit from the loop can only be achieved by powering down the disc drive.

4-15. INTERNAL DIAGNOSTICS

The disc drive internal diagnostics include self-test routines and run time error and fault reporting circuits. The self-test routines, normally activated at power on, consist of a series of subtests which check overall operation of the disc drive. The disc drive must pass all host dependent circuits (unit 2) subtests to come on line. In the event of a device dependent circuits (DDC) subtest failure, the disc drive is allowed to come on line. After power on, run time error and fault reporting circuits in disc drive assembly A1 continually monitor certain operations of the disc drive. Run time errors and faults are logged in the disc drive error logs. Details of these two diagnostic tools are provided in the following paragraphs. Refer to table 4-5 for a summary of the diagnostics.

4-16. SELF TEST

The disc drive can execute self-test diagnostic routines which are programmed into the single board controller device dependent servo system firmware. When the disc drive is powered on, these routines are automatically initiated to perform a series of subtests which verify operation of the disc drive. The subtests perform many hardware checks first by microdiagnostics and then by higher level macrodiagnostics such as seeks, reads, and writes.

Go/no-go test results are indicated by the FAULT/ON LINE indicator on the front panel of the disc drive and details of subtest failures are presented on the Self Test display on the rear panel. The host can determine details of self-test failures using the CS/80 Request Status command. The internal diagnostics can also be initiated at any time by controls on the rear panel of the disc drive or by the host computer using the Initiate Diagnostic command. Details of the diagnostic tests are provided in the following paragraphs.

4-17. SELF-TEST SUBTESTS

The subtests run during self test can be divided into six functional groups. A general description of the tests in each group, listed in the order that they are performed, is provided in the following paragraphs. Refer to tables 4-1 and 4-2 for a listing of the subtests and the failure conditions detected by the tests.

The first group of subtests (01 through 07, table 4-1) checks the operation of the SBC. The subtests include a short checkout of the SBC microprocessor, a checksum of both the EXEC ROM and the an exhaustive write/read test of all of the RAM, a loopback test of the DMA gate array IC, a verification of the timer circuitry, and a test of the HP-IB interface IC. A full set of these subtests is run only when self test is initiated at power on. When self test is initiated by either the SELF TEST switch or the host, then only the timer test, the DMA test, and a limited RAM test are performed. This is to protect the existing runtime environment. The subtests described above check the operation of the IC's, circuits, and interfaces resident in the SBC.

The second group of subtests (0AH through 12H, table 4-2) checks the operation of disc drive functions independent of disc drive assembly A1. These subtests include tests of the SBC device dependent resident IC's and circuits, a checksum of the device specific PROM, and the sensing of the proper 12 volt power.

The third group of subtests (13H through 1CH, table 4-2) checks the operation of disc drive assembly A1 to the extent of servo activity. The disc drive is selected, a restore command is performed and a few seek commands are issued and monitored for proper completion, direction, and pulse count.

The fourth group of subtests (1DH through 25H, table 4-2) performs further checks of the disc drive assembly A1 servo mechanism, and the read function, as far as position sensing. A scan ID command verifies that the sector headers can be read. A more exhaustive sequence of seeks is then executed, both verifying the subsequent location as well as monitoring the speed performance.

The fifth group of subtests (26H through 5EH, table 4-2) checks seek, read, and write, both one and two sectors, at the inner diameter (ID) and the outer diameter (OD). Reads and writes are also performed on every surface.

The sixth group of tests (5FH through 65H, table 4-2) checks out the error and fault detection circuitry. Circuit tests include: ID not found on a scan ID command, underrun condition, a command aborted, and both ECC correctable and uncorrectable errors.

4-18. SELF-TEST ERROR REPORTING

There are three ways which the disc drive reports self-test results to the user. The first way is by means of the front panel FAULT/ON LINE indicator. The second way is via the Self Test display on the rear panel. The third way is by means of the CS/80 Request Status command. The following paragraphs provide details of how these three methods are used to report self-test results.

4-19. FAULT/ON LINE INDICATOR. The red and green LED's which comprise the front panel FAULT/ON LINE indicator signal the operating status of the disc drive. See figure 4-1. A momentary solid red and green display and then a flashing green display occurs when the disc drive is powered on and self test is executing. If the display remains a solid red and green, this means that the single board controller (unit 2) has failed self test. At the end of self test, a solid green display indicates that the disc drive has passed self test and is ready for operation. A solid red display indicates that the disc drive has failed self test. When a self-test failure is indicated, the 2-digit hexadecimal Self Test display should be consulted to determine the source of the failure.

4-20. SELF-TEST DISPLAY. The rear panel 2-digit hexadecimal Self Test display (see figure 4-1) will normally show a pass (**P.X.**) or fail (**F.X.**) indication, with **X.** denoting HP-IB address 0 through 7. When the SELF TEST RESULTS switch is used to toggle out results, the display will show all of the results for unit 0, 1, and 2, one unit at a time, until all of the information has been displayed. Unit 0 is the disc drive, unit 1 is not assigned, and unit 2 is the single board controller.

Note: The "Unit 2" terminology for the single board controller applies only to the disc drive self-test display. The host operating system addresses the controller as unit 15. The "Unit 2" designation for the single board controller is used because the self-test display does not have enough digits to present a U15 readout.

Depending on the subtest failed, the display may indicate more than one failed FRA. In the case of multiple FRA failures, the assemblies will be reported in order of most probable failure. Details of the subtest failed follows the FRA failure information. The following is a summary of the 2-digit readout display.

	FIRST DIGIT	SECOND DIGIT
U. =	Unit number designator	Unit number (0-2) (See figure 4-1)
A. =	Field Replaceable Assy number designator	Field Replaceable Assy number (1-6) (See figure 4-1)

```
P. = Self test pass    HP-IB address (0-7)

F. = Self test fail    HP-IB address (0-7)

0.-6. = Failing        0.-F. = Failing
        self-test              self-test
        subtest                subtest
        number, high           number, low
        digit.                 digit.
        (Refer to              (Refer to
        tables 4-1,            tables 4-1,
        4-2)                   4-2)
```

The following are examples of typical display readout sequences:

- **SELF TEST PASS**

DISPLAY MESSAGE

P.3. Indicates that unit 0 (disc drive) and unit 2 (single board controller) have passed self test. The HP-IB address is set to 3.

- **SELF-TEST FAILURE - UNIT 0 (DISC DRIVE)**

DISPLAY MESSAGE

F.3. Indicates that self test has failed on unit 0 (disc drive) or unit 2 (single board controller). The HP-IB address is set to 3. Press and release the DISPLAY RESULTS switch.

U.0. Indicates that unit 0 (disc drive) is ready to report its results upon subsequent operation of the DISPLAY RESULTS switch. (If unit 0 has passed self test and has no results to report, then the next operation of the switch will change the display to **U.2.** to indicate that unit 2 [single board controller] will be displaying its results next.) Press and release DISPLAY RESULTS switch.

A.4. Indicates that FRA4 (power supply assembly A4) is the most probable cause of the failure.

A.2. Indicates that FRA5 (single board controller PCA-A5) is the second most probable cause of the failure. Push and release DISPLAY RESULTS switch.

1.1. Indicates that subtest 11 has failed. This is defined in table 4-2 as "12V threshold bit (bit 0 of DDC self-test register) not set". Press and release DISPLAY RESULTS switch.

U.2. Indicates that unit 2 (single board controller), will display its results next. Press and release DISPLAY RESULTS switch.

F.3. Indicates that unit 2 has no results to report and the self-test readout cycle is complete.

- **SELF-TEST FAILURE - UNIT 2 (SINGLE BOARD CONTROLLER**

DISPLAY MESSAGE

F.3. Indicates that self test has failed on unit 0 (disc drive) or unit 2 (single board controller). The HP-IB address is set to 3. Press and release the DISPLAY RESULTS switch.

U.2. Indicates that unit 2 (single board controller) has failed self test. Press and release DISPLAY RESULTS switch.

A.5. Indicates that FRA5 (single board controller PCA-A5) is the probable cause of the failure. Push and release DISPLAY RESULTS switch.

0.3. Indicates that subtest 03 has failed. This is defined in table 4-1 as "Test of last 15 kilobytes of RAM failed". Press and release DISPLAY RESULTS switch.

F.3. Indicates that self-test readout cycle is complete.

4-21. REQUEST STATUS. If an Initiate Diagnostic command (DIAG) is issued to the disc drive and an execution message returns a QSTAT of 1, this means that a self-test error has occurred. A Request Status command (REQSTAT) should be issued to get back the reason for the previous QSTAT of 1. When the Request Status command is executed, a 20-byte field is returned. This field is defined in the CS/80 instruction set Programming Manual, part no. 5955-3442. When self test is executed and it fails, the Diagnostic Result Bit (bit 24) will be set in the Fault Error Field (sometimes referred to as the Error Fault Field) of the 20 bytes returned from the Request Status command. When bit 24 is set, P1, P2, P3, P7, and P8 contain specific self-test results, as detailed below:

- P1 - Identifies the most suspect FRA:

  1 = FRA1 (disc drive assembly A1)
  2 = FRA5 (SBC PCA-A5)
  4 = FRA4 (power supply assembly A4)
  5 = FRA5 (SBC PCA-A5)
  6 = Connectors

- P2 - Identifies the next most suspect FRA:

  Same code as P1

- P3 - Failed disc drive (unit 0) self-test subtest. Refer to table 4-2.

- P7 - Failed disc drive error condition. Refer to table 4-3, Disc Drive Error Condition List.

- P8 - Details of failed disc drive error condition. See figure 4-2, P8 Signal Source.

Note: The detailed error condition information given in P8 is obtained from various sources in the disc drive, depending on the test error. In order to identify the reporting source for a particular fault, it is necessary to note the numbers given in P3 (failed self-test subtest) and P7 (disc drive error condition). The point in figure 4-2 where the P3 number (vertical column) and the P7 number (horizontal column) intersect is the reporting source, identified by a letter code. A listing of these codes, together with the information supplied by the identified sources, is provided below.

DE - Data Error Byte

```
LSB 0 = Recoverable
    1 = Marginal
    2 = Marginal (ECC)
    3 = Uncorrectable
MSB 4 = Uncorrectable on write
```

Note: More than one bit may be set. For example, if one location received an uncorrectable error and other locations all had recoverable errors, the data error byte will be set to 09H.

E - Disc Controller IC Error Register

```
LSB 0 = Data address mark not found
    1 = Track 0 error
    2 = Aborted command - Drive not
        ready or write fault
    3 = Unused
    4 = ID not found
    5 = Unused
    6 = CRC error
MSB 7 = Bad block
```

FC - Fault Code List

Refer to table 4-4, Fault Code List.

N - Number of seeks

Specifies the number of seeks performed before failure occurred.

S - Disc Controller IC Status Register

```
LSB 0 = Error bit.
    1 = Command in progress.
    2 = Unused
    3 = DRQ (data request)
    4 = Seek complete
    5 = Write fault
    6 = Drive ready (normally set)
MSB 7 = Busy
```

Z - All zero's. This is a valid subtest number/error condition pairing. However, no additional information is given in P8.

4-22. REQUEST STATUS EXAMPLE. The following example shows how to interpret P1, P2, P3, P7, and P8 returned for a Request Status command following a self-test failure.

P1 = 1
P2 = 2
P3 = 26H
P7 = 3DH
P8 = AEH

P1 and P2 indicate that the most suspect FRA is FRA1 (disc drive assembly A1) and the next most suspect FRA is FRA5 (SBC PCA-A5). P3 indicates that the failed self-test subtest is 26H. This is

defined in table 4-2 as "While attempting to read one sector at the outer diameter, either the seek or the read failed". P7 indicates that the disc error condition is 3DH, defined in table 4-3 as "Unit fault". Using P3 and P7 to identify the P8 signal source shows "FC" as the source. This indicates that table 4-4, Fault Code List, should be consulted. Table 4-4 lists AEH as "Verify position operation reveals drive is on the wrong head" as the fault.

4-23. RUN TIME ERROR AND FAULT REPORTING

The return of a QSTAT of 1 following the issuance of a non self-test command to the disc drive implies that a full status should be requested. A Request Status command should thus be issued to get back the reason for the QSTAT of 1. Assuming that a hardware fault or data error of some kind has occurred, the Diagnostic Result Bit (bit 24) will not be set in the Error Fault Field (Fault Error Field) of the 20 bytes returned from the Request Status command. P7 will contain the disc drive fault code and in certain cases, P8 contains additional information.

P7 - Disc fault code. Refer to table 4-4, Fault Code List.

P8 - If P7 is in the range of 50-6F, P8 is disc controller IC error register (**E**). Refer to paragraph 4-21 for details.

If P7 is in the range of 70-8F, P8 is disc controller IC status register (**S**). Refer to paragraph 4-21 for details.

4-24. EXTERNAL EXERCISER

The CS/80 external exerciser is an interpreter which links the disc drive internal diagnostics to a service-trained person. The *CS/80 External Exerciser Reference Manual,* part no. 5955-3462 describes how the exerciser interfaces to CS/80 devices and includes specific information for the HP 7941 and HP 7945 Disc Drives. The following paragraphs briefly describe the functions of the external exerciser commands.

4-25. AMIGO CLEAR (AMCLEAR)

The AMCLEAR command clears the device on the channel which is currently addressed.

4-26. CANCEL TRANSACTION (CANCEL)

The CANCEL command causes graceful termination of most CS/80 transactions, leaving them in the reporting phase.

4-27. TEST HP-IB CHANNEL (CHANNEL)

The CHANNEL command initiates a read and write loopback test over the HP-IB channel.

4-28. CHANNEL INDEPENDENT CLEAR (CICLEAR)

The CICLEAR command will clear any command connected to the channel.

4-29. CLEAR LOGS (CLEAR LOGS)

The CLEAR LOGS command clears the run-time data error log, the error rate test log, and the fault log.

4-30. DESCRIBE SELECTED UNIT (DESCRIBE)

The DESCRIBE command allows information within the currently addressed unit to be sent to the HP 85.

4-31. PERFORM INTERNAL DIAGNOSTICS (DIAG)

The DIAG command invokes diagnostic routines which reside in the internal device controller firmware. The DIAG command has three parameter bytes. The first two of these bytes are an integer loop count. The third byte is a diagnostic test number. This command may be directed to unit 15 (SBC) or unit 0 (disc drive).

If the command is directed to unit 15, the valid value range for the diagnostic test number parameter is 0 through 3. These values correspond to the following tests:

0 = Full Run Time Self Test. Performs the following three SBC tests as well as the unit 0 self test.

1 = SBC RAM Test. Performs the two pass RAM test on an empty 1k data buffer. RAM allocated to the units and/or the operating system is not tested.

2 = DMA Test. Performs the DMA test run at power-on.

3 = Timer Test. Performs the timer test run at power-on.

If the command is directed to unit 0, the valid value range is also 0 through 3. These values correspond to the following tests:

0 = Unit 0 DDC power-on self test. This does not include the SBC self test; however, the entire power-on DDC self test is performed.

1 = Random Seek Test. A total of 256 seeks are performed per loop.

2 = Full Stroke Seek Test. A total of 256 seeks from outer diameter (OD) to inner diameter (ID) are performed per loop.

3 = Incremental Seek. Performs successive one-track seeks from OD to ID and back again.

4-32. OUTPUT ERROR RATE TEST LOG (ERT LOG)

The ERT LOG command allows access to the error rate test log which contains an accumulation of all read errors which were found during a read-only or write-then-read error rate test. Error rate test errors are accumulated until the log is cleared using the CLEAR LOGS command.

4-33. EXIT PROGRAM (EXIT)

The EXIT command causes the CS/80 external exerciser program to exit.

4-34. OUTPUT FAULT LOG (FAULT LOG)

The FAULT LOG command allows access to the fault log, an accumulation of the faults which have occurred on the disc drive since the last time a CLEAR LOGS command was issued.

4-35. OUTPUT HELP INFORMATION (HELP)

The HELP command prints all of the command names.

4-36. INITIALIZE MEDIA (INIT MEDIA)

The INIT MEDIA utility performs an initialization routine on the disc drive. The INIT MEDIA utility has a valid value of B, P, and I. These values correspond to the following:

B = Initializes the logic region. Spare table, spare tracks, sector headers, and logs are left intact.

P = Initializes the logic region and field spares are deallocated. Factory spares and logs are unchanged.

I = Initializes the entire drive. Logical tracks, spare tracks, and maintenance tracks are cleared. The spare table (factory and field spares) is written back onto the maintenance tracks.

4-37. UPDATE DEVICE LOGS (PRESET)

The PRESET command causes all recent information in controller RAM to be logged on the disc maintenance tracks.

4-38. REQUEST STATUS (REQSTAT)

The REQSTAT utility sends a status message from the device to the exerciser.

4-39. PERFORM READ-ONLY ERROR RATE TEST (RO ERT)

The RO ERT command allows a sequential or random read to take place in order to locate any read errors.

4-40. OUTPUT RUN LOG (RUN LOG)

The RUN LOG command allows access to the run log which contains an accumulation of all read errors which were found during run time. Run-time data errors are accumulated until the log is cleared using the CLEAR LOGS command.

4-41. SPARE (SPARE)

The SPARE utility physically relocates a track to an address which is reserved for sparing.

4-42. OUTPUT SPARE TABLE (SPARE TABLE)

The SPARE TABLE command accesses the information in the spare table.

4-43. OUTPUT DEVICE TABLE (TABLES)

The TABLES command accesses the tables stored internally within the device in order to determine the operational status of the device.

4-44. PERFORM SERVO TEST (SERVO)

The SERVO test checks the operation of the servo system. An exhaustive sequence of seeks is executed verifying the subsequent location as well as monitoring the speed performance. The entire sequence of seeks is repeated six times.

4-45. SET UNIT NUMBER (UNIT)

The UNIT utility allows the user to select the unit number to be addressed within the device. The disc drive is unit 0.

4-46. PERFORM WRITE-THEN-READ ERROR RATE TEST (WTR ERT)

The WTR ERT command writes a predefined data pattern over a specified area of the disc, then reads all data which was written.

4-47. TROUBLESHOOTING

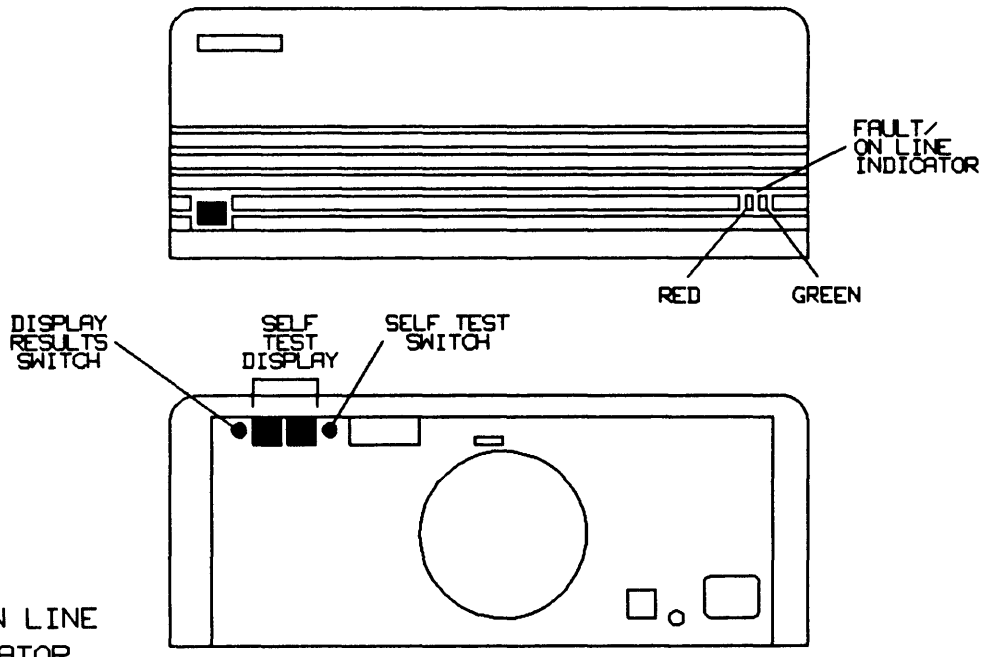
When troubleshooting the disc drive, the first thing to do is to determine if the fault is repeatable or intermittent. A repeatable fault usually causes the same self-test fail result to be presented each time self test is performed. An intermittent fault, on the other hand, occurs at random intervals, and may not always cause a self-test failure.

In the case of a repeatable fault, self test will identify the failing FRA with a 95 percent certainty. In the event that more that one FRA is listed as the possible cause of the failure, replace the FRA's, one at a time, in the order given in the self-test display.

Note: Cable faults (an open cable conductor, loose cable connector, etc.) may present a multiple FRA failure message. The FRA's listed will be the FRA's at either end of the defective cable. All cabling should therefore be checked before replacing any FRA's.

Note: Cables W1 and W3 are sufficiently long to allow FRA1 (disc drive assembly A1) to be connected into circuit adjacent to the disc drive cabinet. This allows a substitute FRA1 to be connected into circuit without removing FRA1 from the cabinet.

Attempt to isolate the fault to a specific FRA by running self test following the replacement of each FRA.



FAULT/ON LINE INDICATOR

RED	GREEN	
ON	ON	INDICATOR TEST FOR 1 SECOND AFTER INITIATING SELF TEST OR CONTROLLER (U2) FAILED SELF TEST.
OFF	FLASHING	EXECUTING SELF TEST OR DISC DRIVE ACTIVE.
OFF	ON	DISC DRIVE PASSED SELF TEST OR DISC DRIVE INACTIVE.
ON	OFF	DISC DRIVE FAILED SELF TEST;READY FOR DIAGNOSTICS
ON	FLASHING	DISC DRIVE FAILED SELF TEST;TEST ROUTINES STILL ACTIVE.

SELF TEST DISPLAY

DISPLAY	MESSAGE	
8.8.	DISPLAY TEST	GO/NO-GO TEST RESULT
P.*	SELF TEST PASS. *=HP-IB ADDRESS	
F.*	SELF TEST FAIL. *=HP-IB ADDRESS	
rd	RELEASE DENIED	
U.0.	UNIT 0 (DISC DRIVE)	UNIT FAILED
U.2.	UNIT 2 (SINGLE BOARD CONTROLLER)	
A.1.	DISC DRIVE FRA1	FIELD REPLACEABLE ASSEMBLY (FRA) FAILED
A.2.	SBC FRA5	
A.4.	POWER SUPPLY FRA4	
A.5.	SBC FRA5	
A.6.	CONNECTORS	
0.0.	UNIT 0/ UNIT 2 SELF-TEST SUBTEST FAILED SEE TABLES 4-1 AND 4-2 FOR LISTINGS	
6.1.		
8.8.		

FILE=S7945A07

Figure 4-1. Self-Test Controls and Readout

Table 4-1. Single-Board Controller (Unit 2) Self-Test Subtest List

READOUT (HEX)	SUBTEST
	GROUP 1
88	Microprocessor failed.
01	Test of the first 1 kilobyte of RAM failed.
02	Checksum of EXEC ROM failed.
03	Test of last 15 kilobyte of RAM failed.
04	DMA machine test failed.
05	SBC timer circuitry not within specification.
06	HP-IB interface test failed.
07	Configuration failure - cannot find a valid unit 0.

Table 4-2. Disc Drive (Unit 0) Self-Test Subtest List

READOUT (HEX)	SUBTEST
	GROUP 2
0A	PUPO register written and was 0FH when read back.
0B	Value read from PUPO register was not value written.
0C	DMA loopback test failed transfer into DMA RAM.
0D	DMA loopback test failed transfer out of DMA RAM.
0E	Write to 2^3 head select line did not set head bit 3 (bit 1 of DDC self-test register).
0F	Write to 2^3 head select line did not clear head bit 3 (bit 1 of DDC self-test register).
10	Device specific PROM read into RAM - subsequent checksum failed.
11	12 volt threshold bit (bit 0 of DDC self-test register) not set.
12	Value read from a disc controller IC register not value written.
	GROUP 3
13	Timeout occurred after drive selected while waiting for drive ready status.
14	Restore Command issued and failed.
15	Seek completed, seek complete bit is not set in the disc controller IC status, but is set in bit 3 of DDC self-test register.
16	Seek command completed, Seek complete not set in either disc controller IC status or the self-test register.
17	Seek command failed, disc controller IC status register indicates reason.
18	Seek command failed, disc controller IC error register indicates reason.
19	Seek completed, but pulse count was not 1, as expected.
1A	Seek completed, but pulse count was not 15 as expected.
1B	Seek completed, but the direction bit (bit 2 of the DDC self-test register) did not indicate it.
1C	Seek completed, but the direction bit did not indicate out.

Table 4-2. Disc Drive (Unit 0) Self-Test Subtest List (Continued)

READOUT (HEX)	SUBTEST
	GROUP 4
1D	Scan ID failed due to data error.
1E	Scan ID failed, reason indicated in disc controller IC status register.
1F	Scan ID failed, reason indicated in disc controller IC error register.
20	A seek failed in the seek test, command did not complete.
21	A seek failed in the seek test, command completed - but no seek complete status.
22	A seek failed in the seek test, command completed in failure.
23	A Scan ID failed in the seek test.
24	A Scan ID in the seek test indicates that the drive is on the wrong track.
25	Was not able to complete all the seeks in the seek test within the allotted time.
	GROUP 5
26	While attempting to read one sector at the outer diameter, either the seek or the read failed.
27	While attempting a write then read of one sector at the OD, either the seek or the write failed.
28	While attempting a write then read of one sector at the OD, either the read failed, or the data read did not match that written.
29	While attempting a write then read of one sector on surface 0, either the seek of the write failed.
2A	While attempting a write and then read of one sector on surface 0, either the read failed, or the data read did not match that written.
2B	After a successful write then read of one sector on every surface (with a unique pattern for each surface), test produced a seek failure, a read failure, or data different from that written.
2C	While attempting a write then read of one sector on surface 1, either the seek of the write failed.
2D	While attempting a write and then read of one sector on surface 1, either the read failed, or the data read did not match that written.

Table 4-2. Disc Drive (Unit 0) Self-Test Subtest List (Continued)

READOUT (HEX)	SUBTEST
2E	After a successful write then read of one sector on every surface (with a unique pattern for each surface), test produced a seek failure, a read failure, or data different from that written.
2F	While attempting a write then read of one sector on surface 2, either the seek of the write failed.
30	While attempting a write and then read of one sector on surface 2, either the read failed, or the data read did not match that written.
31	After a successful write then read of one sector on every surface (with a unique pattern for each surface), test produced a seek failure, a read failure, or data different from that written.
32	While attempting a write then read of one sector on surface 3, either the seek of the write failed.
33	While attempting a write and then read of one sector on surface 3, either the read failed, or the data read did not match that written.
34	After a successful write then read of one sector on every surface (with a unique pattern for each surface), test produced a seek failure, a read failure, or data different from that written.
35	While attempting a write then read of one sector on surface 4, either the seek of the write failed.
36	While attempting a write and then read of one sector on surface 4, either the read failed, or the data read did not match that written.
37	After a successful write then read of one sector on every surface (with a unique pattern for each surface), test produced a seek failure, a read failure, or data different from that written.
38	While attempting a write then read of one sector on surface 5, either the seek of the write failed.
39	While attempting a write and then read of one sector on surface 5, either the read failed, or the data read did not match that written.
3A	After a successful write then read of one sector on every surface (with a unique pattern for each surface), test produced a seek failure, a read failure, or data different from that written.
3B	While attempting a write then read of one sector on surface 6, either the seek of the write failed.
3C	While attempting a write and then read of one sector on surface 6, either the read failed, or the data read did not match that written.

Table 4-2. Disc Drive (Unit 0) Self-Test Subtest List (Continued)

READOUT (HEX)	SUBTEST
3D	After a successful write then read of one sector on every surface (with a unique pattern for each surface), test produced a seek failure, a read failure, or data different from that written.
3E thru 55	Reserved for future use.
56	While attempting to read two sectors at the OD, either the seek or the read failed.
57	While attempting a write then read of two sectors at the OD, either the seek or the write failed.
58	While attempting a write then read of two sectors at the OD, either the read failed, or the data read did not match that written.
59	While attempting to read one sector at the inner diameter (ID), either the seek or the read failed.
5A	While attempting a write then read of one sector at the ID, either the seek or the write failed.
5B	While attempting a write then read of one sector at the ID, either the read failed, or the data read did not match that written.
5C	While attempting to read two sectors at the ID, either the seek or the read failed.
5D	While attempting a write then read of two sectors at the ID, either the seek or the write failed.
5E	While attempting a write then read of two sectors at the ID, either the read failed, or the data read did not match that written.
	GROUP 6
5F	A read command was issued for a non-existant sector. The expected ID not found error was not detected.
60	A read was performed with the DMA disabled. The expected overrun in condition was not detected.
61	The drive was deselected and a seek command issued. The expected command aborted status was not detected.
62	ECC correctable test, write full operation failed.
63	ECC correctable test, read operation failed or the data was miscorrected.
64	ECC uncorrectable test, write full operation failed.

Table 4-2. Disc Drive (Unit 0) Self-Test Subtest List (Continued)

READOUT (HEX)	SUBTEST
65	ECC uncorrectable test, read operation failed or value read indicated that correction was attempted.
66	Product number, cannot be read.
67	Product number, value read was unitialized.
68	Product number, wrong number.

Table 4-3. Disc Drive Error Condition List

READOUT (HEX)	ERROR CONDITION
30	Miscompare.
31	Failed.
32	Passed second scan ID on different head.
33	Data errors occurred on every location.
34	Seek timeout - disc controller IC has not completed command.
35	Seek timeout - Command completed - seek complete bit not set.
36	Seek - write fault.
37	Seek - drive not ready.
38	Seek fault.
39	R/W data byte count invalid.
3A	Command aborted.
3B	Disc controller IC timeout - reset.
3C	Disc controller IC timeout - cannot reset.
3D	Unit fault.
3E	Fault occurred, but unable to identify condition.
3F	Verify position failure.

P3

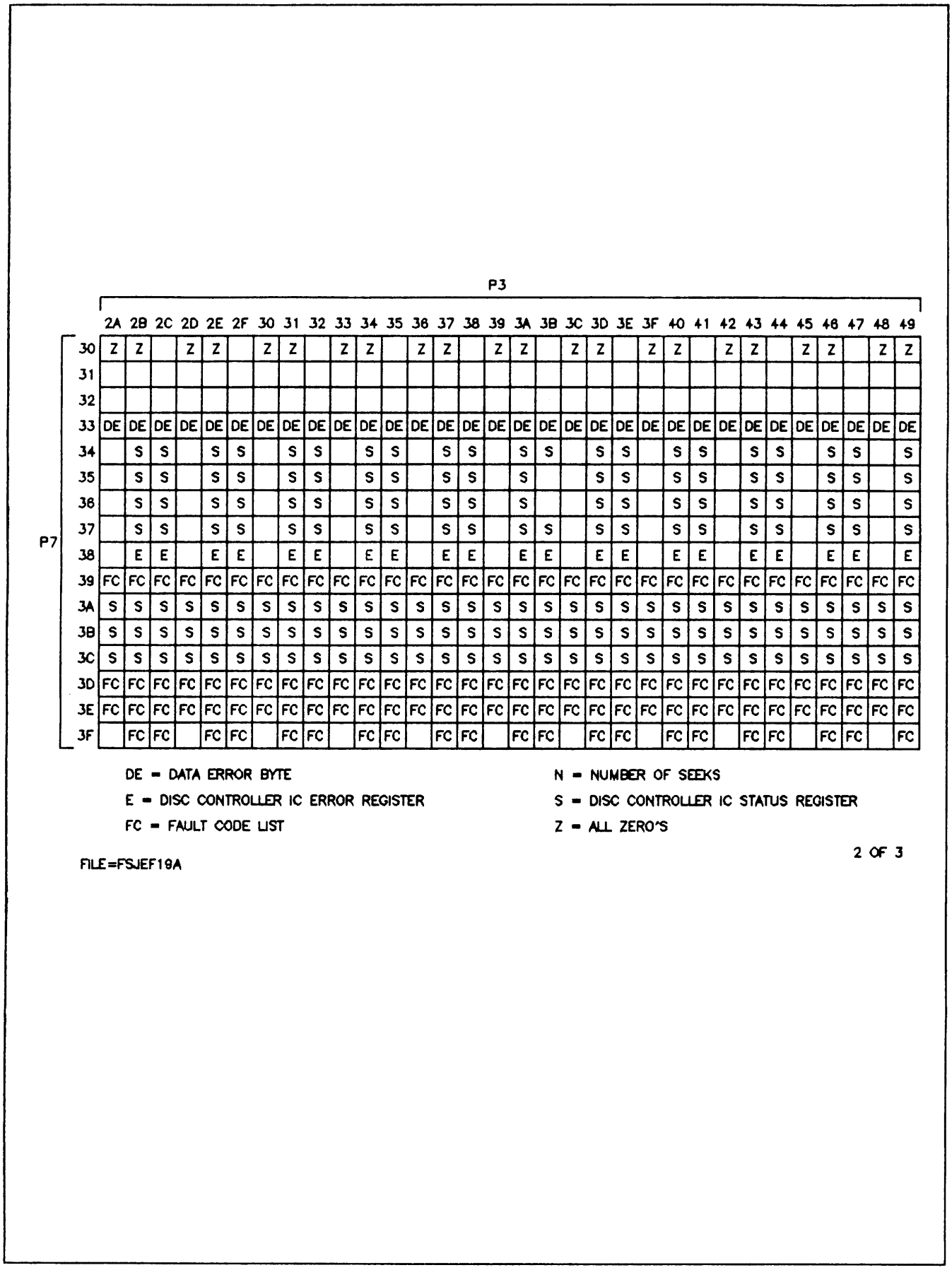
P7	0A	0B	0C	0D	0E	0F	10	11	12	13	14	15	16	17	18	19	1A	1B	1C	1D	1E	1F	20	21	22	23	24	25	26	27	28	29
30	Z	Z	Z	Z					Z																		Z				Z	
31					Z	Z	Z	Z		Z	E	Z	Z	S	E	Z	Z	Z	Z	E	S	FC				FC		N				
32																				E	S	FC										
33																													DE	DE	DE	DE
34														S									N						S	S		S
35											S													N					S	S		S
36																									S				S	S		S
37																									S				S	S		S
38																									E				E	E		E
39																													FC	FC	FC	FC
3A											S																		S	S	S	S
3B											S																		S	S	S	S
3C											S																		S	S	S	S
3D											E																		FC	FC	FC	EC
3E																									FC				FC	FC	FC	FC
3F																													FC	FC		FC

DE = DATA ERROR BYTE
E = DISC CONTROLLER IC ERROR REGISTER
FC = FAULT CODE LIST
N = NUMBER OF SEEKS
S = DISC CONTROLLER IC STATUS REGISTER
Z = ALL ZERO'S

1 OF 3

FILE=FSJEF18A

Figure 4-2. P8 Signal Source (Sheet 1 of 3)



P3

P7	2A	2B	2C	2D	2E	2F	30	31	32	33	34	35	36	37	38	39	3A	3B	3C	3D	3E	3F	40	41	42	43	44	45	46	47	48	49
30	Z	Z		Z	Z		Z	Z		Z	Z		Z	Z		Z	Z		Z	Z		Z	Z		Z	Z		Z	Z		Z	Z
31																																
32																																
33	DE	DE	DE	DE	DE	DE	DE	DE	DE	DE	DE	DE	DE	DE	DE	DE	DE	DE	DE	DE	DE	DE	DE	DE	DE	DE	DE	DE	DE	DE	DE	DE
34		S	S		S	S		S	S		S	S		S	S		S	S		S	S		S	S		S	S		S	S		S
35		S	S		S	S		S	S		S	S		S	S		S			S	S		S	S		S	S		S	S		S
36		S	S		S	S		S	S		S	S		S	S		S			S	S		S	S		S	S		S	S		S
37		S	S		S	S		S	S		S	S		S	S		S	S		S	S		S	S		S	S		S	S		S
38		E	E		E	E		E	E		E	E		E	E		E	E		E	E		E	E		E	E		E	E		E
39	FC	FC	FC	FC	FC	FC	FC	FC	FC	FC	FC	FC	FC	FC	FC	FC	FC	FC	FC	FC	FC	FC	FC	FC	FC	FC	FC	FC	FC	FC	FC	FC
3A	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S
3B	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S
3C	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S
3D	FC	FC	FC	FC	FC	FC	FC	FC	FC	FC	FC	FC	FC	FC	FC	FC	FC	FC	FC	FC	FC	FC	FC	FC	FC	FC	FC	FC	FC	FC	FC	FC
3E	FC	FC	FC	FC	FC	FC	FC	FC	FC	FC	FC	FC	FC	FC	FC	FC	FC	FC	FC	FC	FC	FC	FC	FC	FC	FC	FC	FC	FC	FC	FC	FC
3F		FC	FC		FC	FC		FC	FC		FC	FC		FC	FC		FC	FC		FC	FC		FC	FC		FC	FC		FC	FC		FC

DE = DATA ERROR BYTE
E = DISC CONTROLLER IC ERROR REGISTER
FC = FAULT CODE LIST
N = NUMBER OF SEEKS
S = DISC CONTROLLER IC STATUS REGISTER
Z = ALL ZERO'S

2 OF 3

FILE=FSJEF19A

Figure 4-2. P8 Signal Source (Sheet 2 of 3)

P3

P7	4A	4B	4C	4D	4E	4F	50	51	52	53	54	55	56	57	58	59	5A	5B	5C	5D	5E	5F	60	61	62	63	64	65	66	67	68
30		Z	Z		Z	Z		Z	Z		Z	Z			Z			Z			Z					Z		Z			Z
31																						Z	Z	Z		FC		FC		Z	
32																															
33	DE	DE	DE	DE	DE	DE	DE	DE	DE	DE	DE	DE	DE	DE	DE	DE	DE	DE	DE	DE	DE		E		DE	DE	DE	DE			
34	S		S	S		S	S		S	S		S	S	S		S	S		S	S			S		S						
35	S		S	S		S	S		S	S		S	S	S		S	S		S	S			S		S						
36	S		S	S		S	S		S	S		S	S	S		S	S		S	S			S		S						
37	S		S	S		S	S		S	S		S	S	S		S	S		S	S			S		S						
38	E		E	E		E	E		E	E		E	E	E		E	E		E	E			E		E						
39	FC	FC	FC	FC	FC	FC	FC	FC	FC	FC	FC	FC	FC	FC	FC	FC	FC	FC	FC	FC	FC				FC	FC	FC	FC			
3A	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S		S		S	S	S	S			
3B	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S		S		S	S	S	S			
3C	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S		S		S	S	S	S			
3D	FC	FC	FC	FC	FC	FC	FC	FC	FC	FC	FC	FC	FC	FC	FC	FC	FC	FC	FC	FC	FC				FC	FC	FC	FC	Z		
3E	FC	FC	FC	FC	FC	FC	FC	FC	FC	FC	FC	FC	FC	FC	FC	FC	FC	FC	FC	FC	FC		FC		FC	FC	FC	FC			
3F	FC		FC	FC		FC	FC		FC	FC		FC	FC	FC		FC	FC		FC	FC			FC		FC						

DE = DATA ERROR BYTE

E = DISC CONTROLLER IC ERROR REGISTER

FC = FAULT CODE LIST

N = NUMBER OF SEEKS

S = DISC CONTROLLER IC STATUS REGISTER

Z = ALL ZERO'S

3 OF 3

FILE=FSJEF20A

Figure 4-2. P8 Signal Source (Sheet 3 of 3)

Table 4-4. Fault Code List

Oct	Dec	Hex	Miscellaneous Errors Caused by Externally Initiated Operations
00	00	00	No error.
01	01	01	End of volume.
02	02	02	Power on.
03	03	03	Address bounds error.
04	04	04	Low on spare tracks.
05	05	05	Spare table overflow.
06	06	06	Parameter bounds error on a utility.
07	07	07	Maintenance track overflow - logs are full. (or sector count has overflowed).
			Data Errors
40	32	20	Recoverable data error.
41	33	21	Marginal data error - more than one try recovered the data.
42	34	22	Marginal data error - correction operation was used to recover the data.
43	35	23	Uncorrectable data error.
44	36	24	Recoverable data error - ID field.
45	37	25	Marginal - ID field.
47	39	27	Unrecoverable - ID field.
50	40	28	Recoverable - data address mark not found.
51	41	29	Marginal - data address mark not found.
53	43	2B	Unrecoverable - data address mark not found.
57	47	2F	Unrecoverable data error on write operation (ID field not readable).
			General faults that don't map to a specific status error bit. **Self Test Errors**
60	48	30	Miscompare.
61	49	31	Failed.
62	50	32	Passed second scan ID on different head.
63	51	33	Data error occurred on every location.
64	52	34	Seek timeout - disc controller IC has not completed command.
65	53	35	Seek/Restore timeout - no seek complete.
66	54	36	Seek - write fault.
67	55	37	Seek - drive not ready.
70	56	38	Seek fault.
71	57	39	R/W DMA byte count invalid.
72	58	3A	Write fault - drive not ready.
73	59	3B	Disc controller IC timeout - reset.
74	60	3C	Disc controller IC timeout - cannot reset.
75	61	3D	Unit fault.
76	62	3E	Fault occurred, but unable to identify condition.
77	63	3F	Verify position failure.

Table 4-4. Fault Code List (Continued)

Oct	Dec	Hex	Controller Faults
100	64	40	
101	65	41	Memo sequence error.
102	66	42	No empty memos available.
103	67	43	Too many commands queued.
115	77	4D	Bad execution vector from decoder.
116	78	4E	Byte - underrun bit of DDC errors register set.
117	79	4F	DMA-In. Wrong byte count (DMA never completed). DMA-Out. Wrong byte count (DMA never completed).
			Unit Faults with Disc Controller IC Error Register (Refer to "E - Disc Controller IC Error Register", paragraph 4-21, on how to interpret the P8 error byte.)
121	81	51	Unit fault during read or write.
123	83	53	Unit fault during scan ID.
124	84	54	Unit fault during verify operation.
125	85	55	Unit fault during correction operation.
126	86	56	Retries exhausted on full sector operation.
134	92	5C	Track 000 error on restore.
135	93	5D	Unit fault on restore.
136	94	5E	Format - unit fault.
137	96	5F	Unit fault during seek operation.
			Unit faults with Disc Controller IC Status Register (Refer to "S - Disc Controller IC Status Register", paragraph 4-21, on how to interpret the P8 status byte.)
160	112	70	Write fault on retry of Seek
161	113	71	Drive not ready on retry of Seek
162	114	72	Seek retry fault
163	115	73	Scan ID failed before retry of Seek
164	116	74	Seek timeout fault - 3 seconds
165	117	75	Seek retried
166	118	76	Seek retry timed out - 300 msec
200	128	80	Format - write fault.
201	129	81	Unit fault during read or write.
202	130	82	Aborted command on read or write.
203	131	83	Disc controller IC timeout on read or write. IC has been reset.
204	132	84	Disc controller IC timeout on read or write. IC will not reset.
205	133	85	Disc controller IC timeout during verify.
206	134	86	Disc controller IC timeout during scan ID command.
207	135	87	Disc controller IC timeout during seek.
210	136	88	Disc controller IC timeout during correction.
211	137	89	Drive not ready or write fault on restore.
212	138	8A	Restore completed but no seek complete.
213	139	8B	Restore - disc controller IC timeout - disc controller IC reset.
214	140	8C	Drive not ready on seek.
215	141	8D	Write fault on seek.
216	142	8E	Restore - disc controller IC timeout - disc controller IC will not reset.

Table 4-4. Fault Code List (Continued)

Oct	Dec	Hex	Unit Faults
220	144	90	Read spare table timeout.
221	145	91	Format - Sector count register not zero.
222	146	92	Format - DMA transfer count not valid.
223	147	93	Format - timeout.
224	148	94	Infinite loop detected in logical address mapping - Spare tables lost.
225	149	95	Spare tables read failure
226	150	96	Store spare tables failure.
227	151	97	Read serial number failure.
230	152	98	Write serial number failure.
236	158	9E	Track sparing failed - spare tables lost.
237	159	9F	Zeroing of spare tracks operation failed in Deallocate Spares.
240	160	A0	Seek to deallocated spare failed in Deallocate Spares.
241	161	A1	Copy of track to be spared has failed.
242	162	A2	Write of spare track failed, spare allocated but not assigned.
243	163	A3	Track Sparing cannot obtain resources.
244	164	A4	Track Sparing failed while writing spare tables to disc.
245	165	A5	Verify failed on second spare track.
246	166	A6	Seek failure during verify of spare tracks.
247	167	A7	Disc controller IC error bit set but no error found.
250	168	A8	Write fault during operation other than write (Write current present in head.)
252	170	AA	Disc controller IC overran the DMA (IC register must have glitched).
253	171	AB	Seek Complete will not come true after a write fault.
255	173	AD	ID-not found on scan ID command. Restore performed.
256	174	AE	Verify position operation reveals drive is on the wrong head.
257	175	AF	Verify position operation reveals drive is on the wrong cylinder.
266	182	B6	Write retries on this sector exhausted - due to write fault.
300	192	C0	Unit fault - logs unreadable.

Table 4-5. Diagnostic Summary

UNIT 0 AND UNIT 2 SELF TEST

SELF TEST

1. 78 Subtests. Subtests indicated on rear panel 2-digit hexadecimal display
   Subtest code range: 0A-68H (unit 0), 00-07, 88 (unit 2).

2. 16 supplementary error condition codes. Error code range; 30-3F.

SELF TEST REPORTING, UNIT 0 and UNIT 2

1. Front panel FAULT/ON LINE indicator: pass/fail.

2. Rear panel 2-digit hexadecimal readout:
   - Failed unit.
   - Failed FRA(s).
   - Failed subtest.

SELF TEST REPORTING, UNIT 0

1. QSTAT=1

2. REQUEST STATUS message format:
   - Bit 24 set
   - P1: Most likely failed FRA
   - P2: Second most likely failed FRA
   - P3: Failed subtest
   - P7: Failed error condition
   - P8: Supplementary error codes - data error byte, disc controller IC error register, fault code list, number of seeks, and disc controller IC status register.

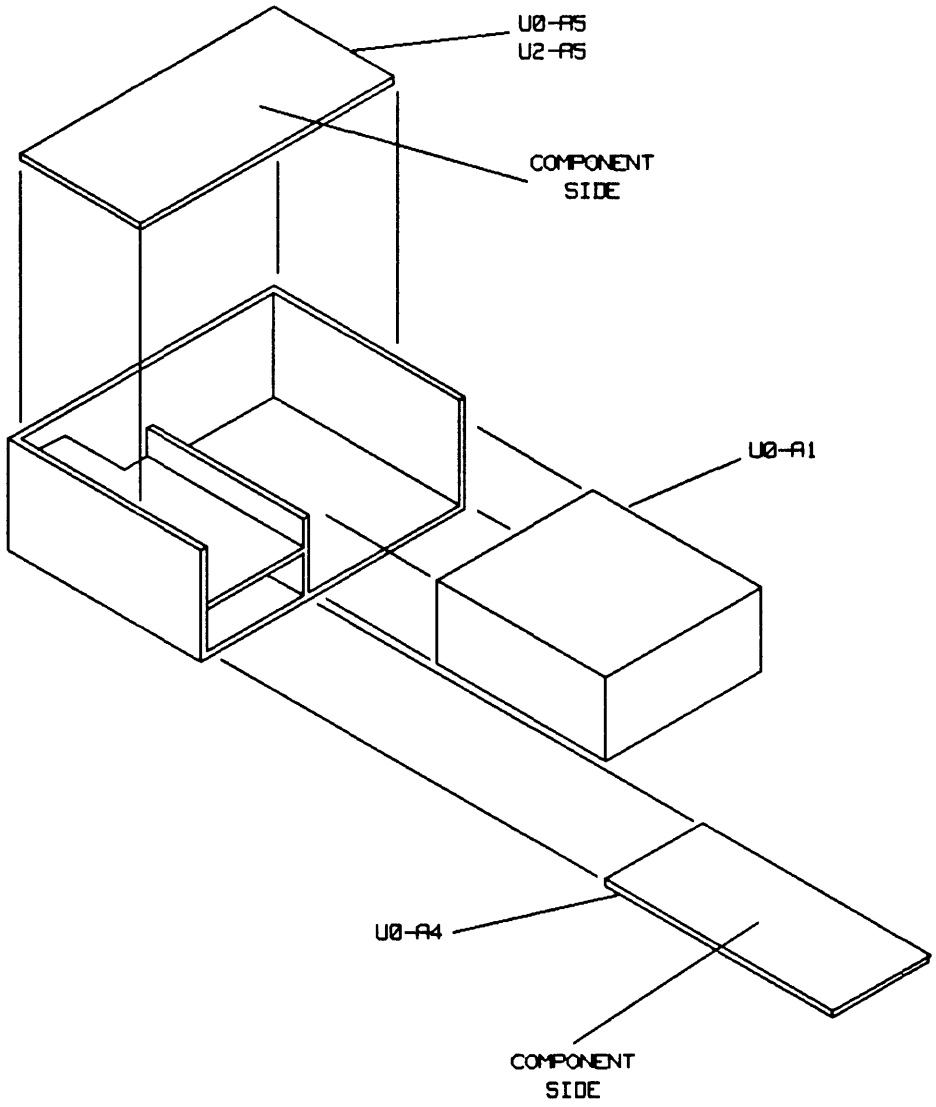
UNIT 0 RUN TIME ERROR AND FAULT REPORTING

RUN TIME ERROR AND FAULT REPORTING

1. QSTAT=1.

2. REQUEST STATUS message format:
   - Bit 24 not set.
   - P7: Fault code list
   - P8: Supplementary error codes - disc controller IC error and status registers.

3. Log entries
   - All faults/data error codes logged in fault log/data error log.
   - Data error address, status byte occurrence count logged in run log.



U (unit)	A (field replaceable assembly)
0-DISC DRIVE	1-DISC DRIVE A1 5-SINGLE BOARD CONTROLLER PCA-A5 4-POWER SUPPLY A4 6-CONNECTORS (NOT SHOWN)
2-CONTROLLER	5-SINGLE BOARD CONTROLLER PCA-A5

FILE=S7945A09

Figure 4-3. Field Replaceable Assembly (FRA) Locations

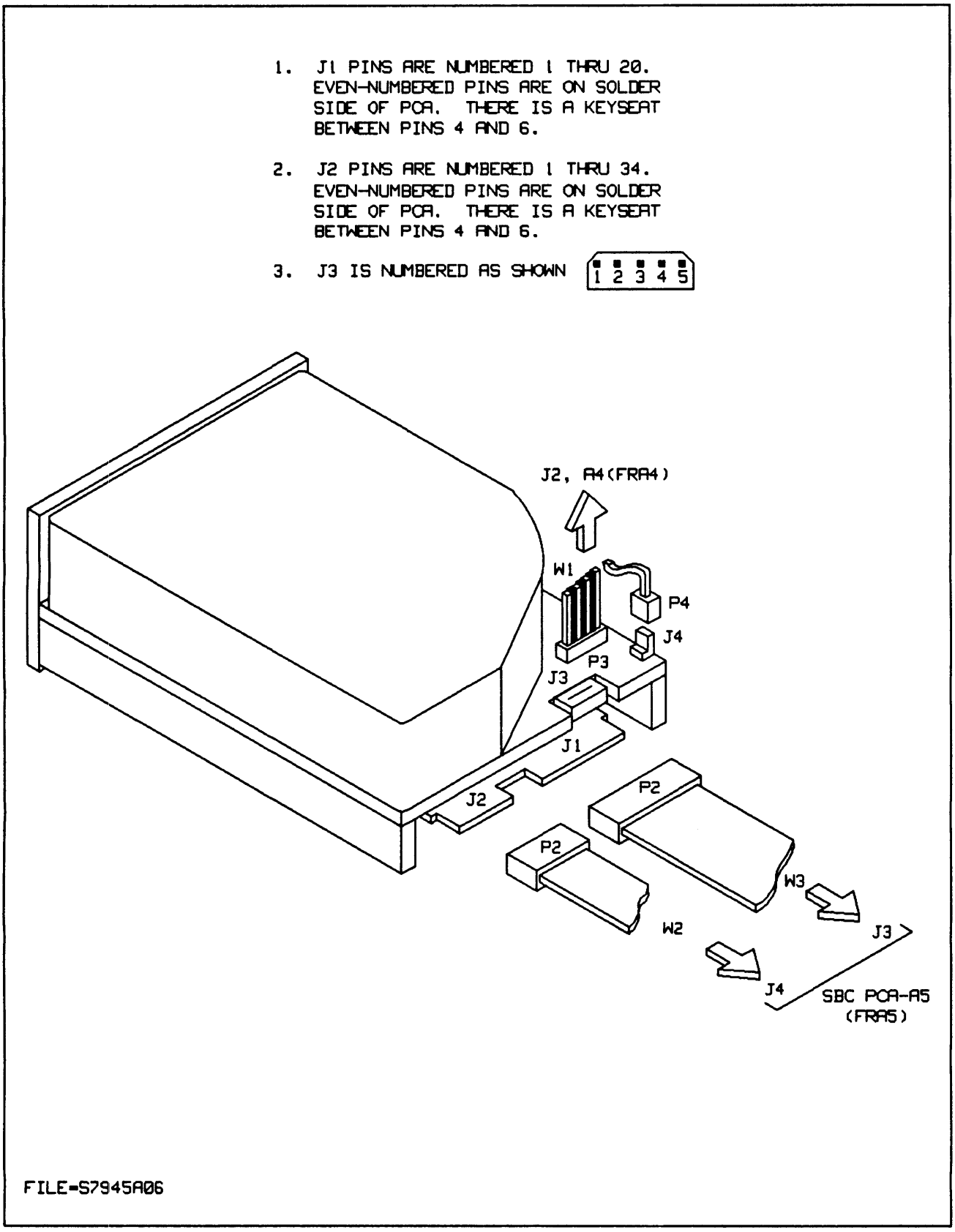


Figure 4-4. FRA1 (Disc Drive A1), Layout and Cable Connections

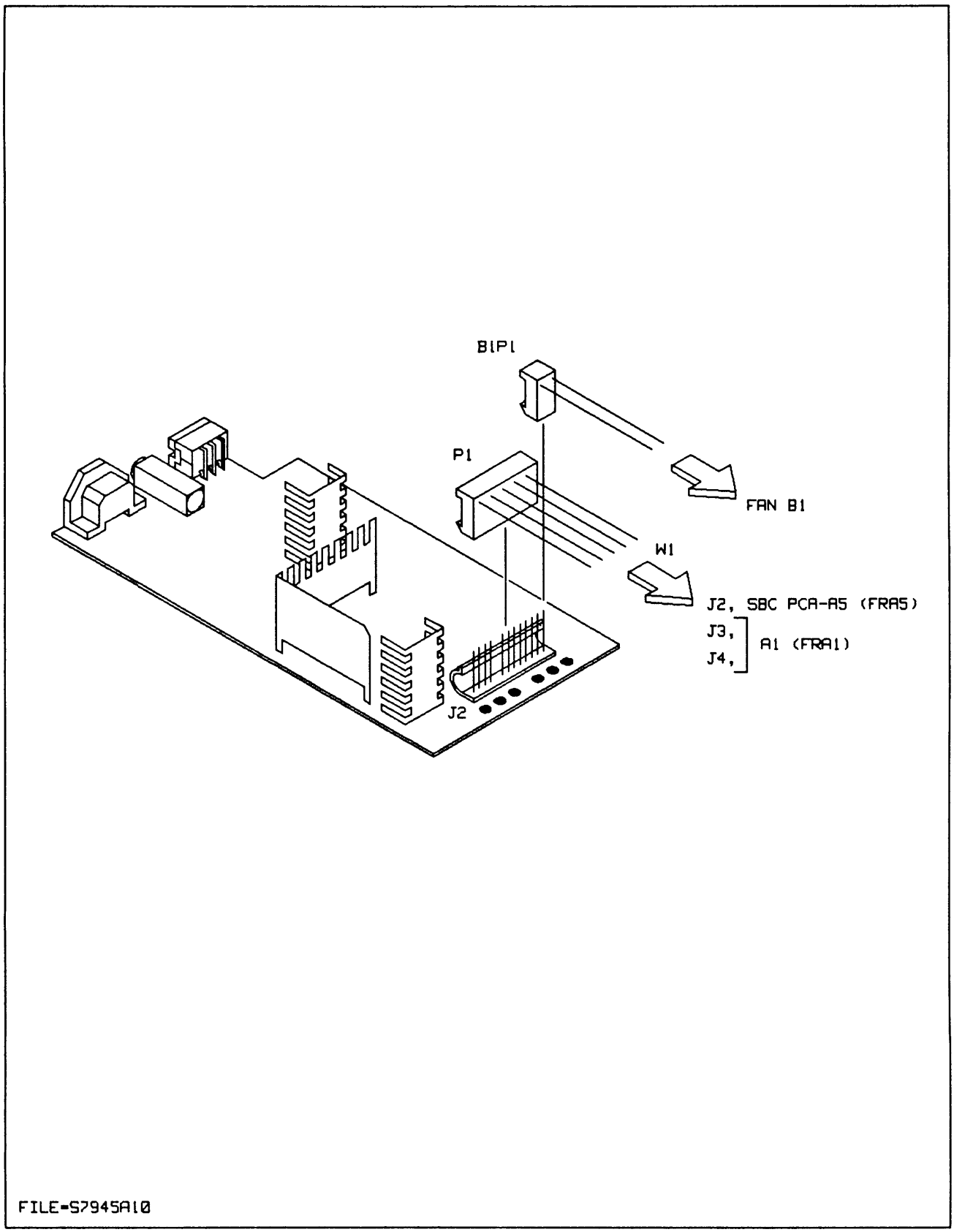


Figure 4-5. FRA4 (Power Supply A4), Layout and Cable Connections

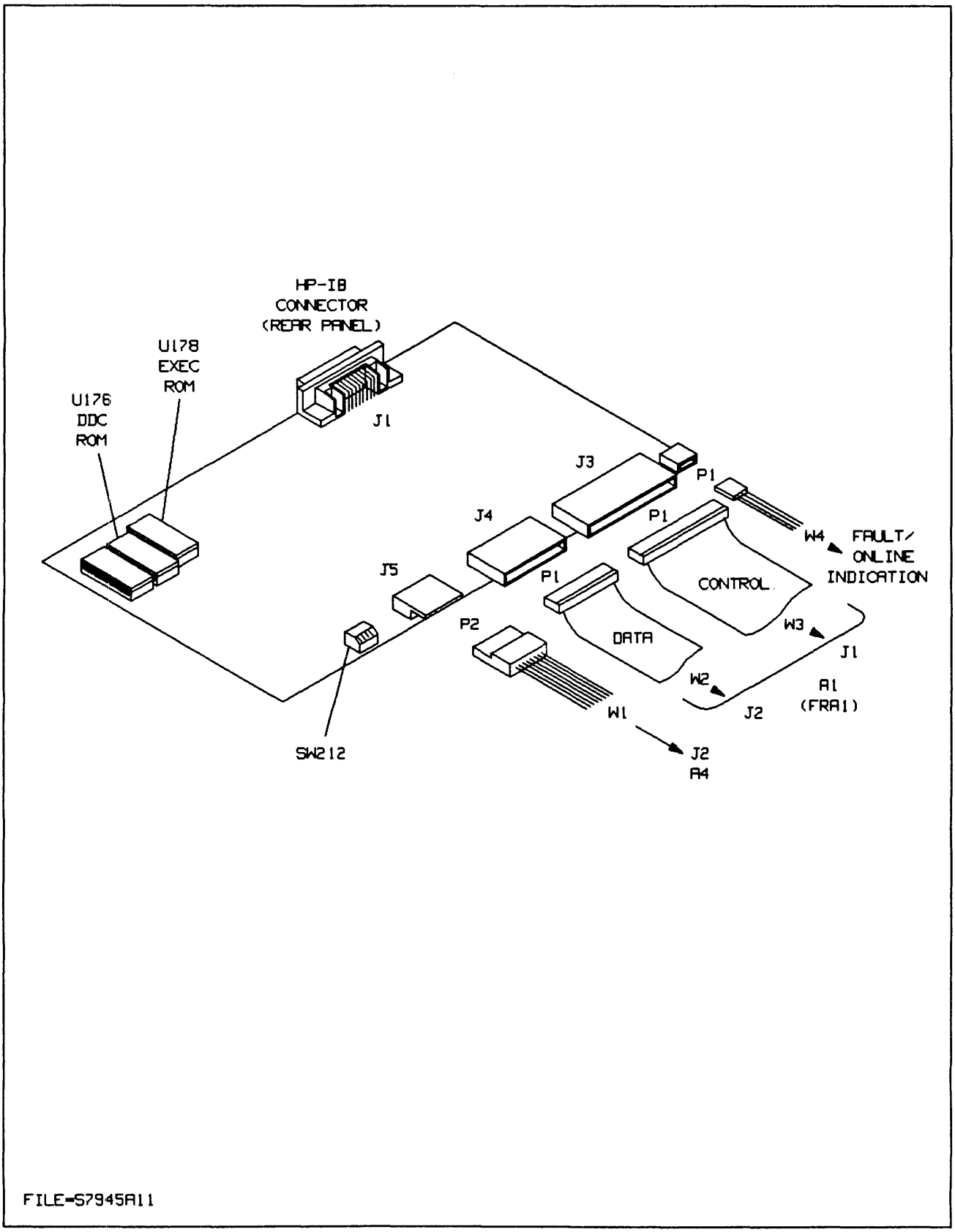
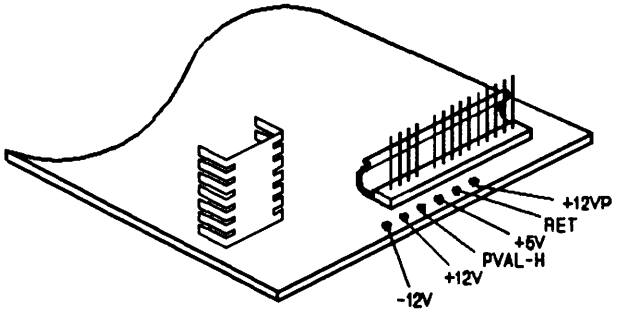


Figure 4-6. FRA5 (SBC PCA-A5), Layout and Cable Connections



TEST POINT	VOLTAGE RANGE
-12V	-11.4 TO -12.6V
+12V	+11.64 TO +12.36V
PVAL-H	≥ +2.4V (TYPICALLY 4.0V)
+5V	+4.85 TO 5.15V
+12VP	11.0 TO 13.0V

NOTE:
1. -12V IS NOT USED IN THE HP7941 AND HP7945.
2. USE RET TEST POINT FOR VOLTMETER RETURN.
3. THE OUTPUT VOLTAGES ARE NOT ADJUSTABLE.
4. MAXIMUM RIPPLE:
   5V SUPPLY: <50mV P-P
   12V SUPPLIES: <100mV P-P

Figure 4-7. FRA4 (Power Supply A4), Test Points and Voltages

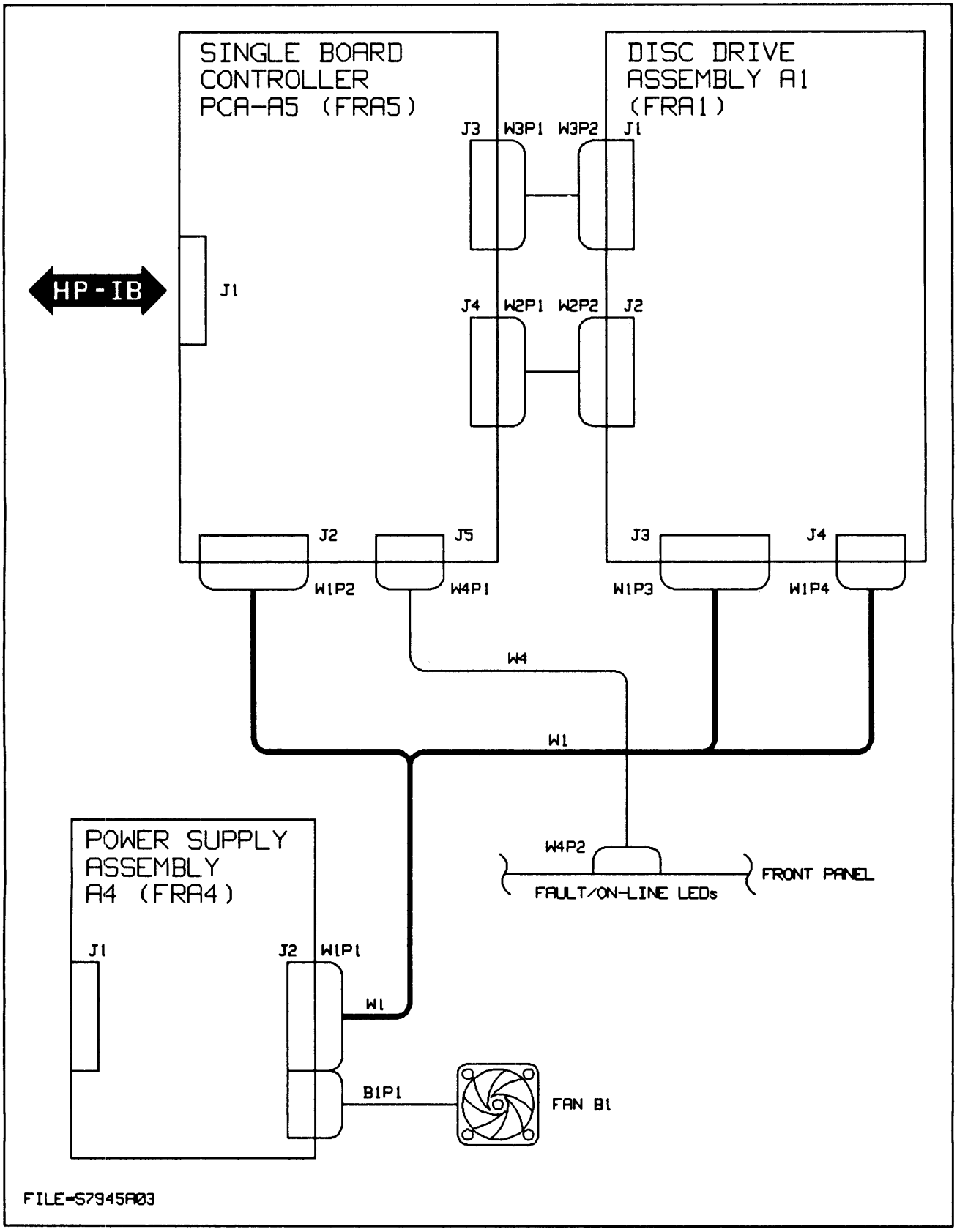
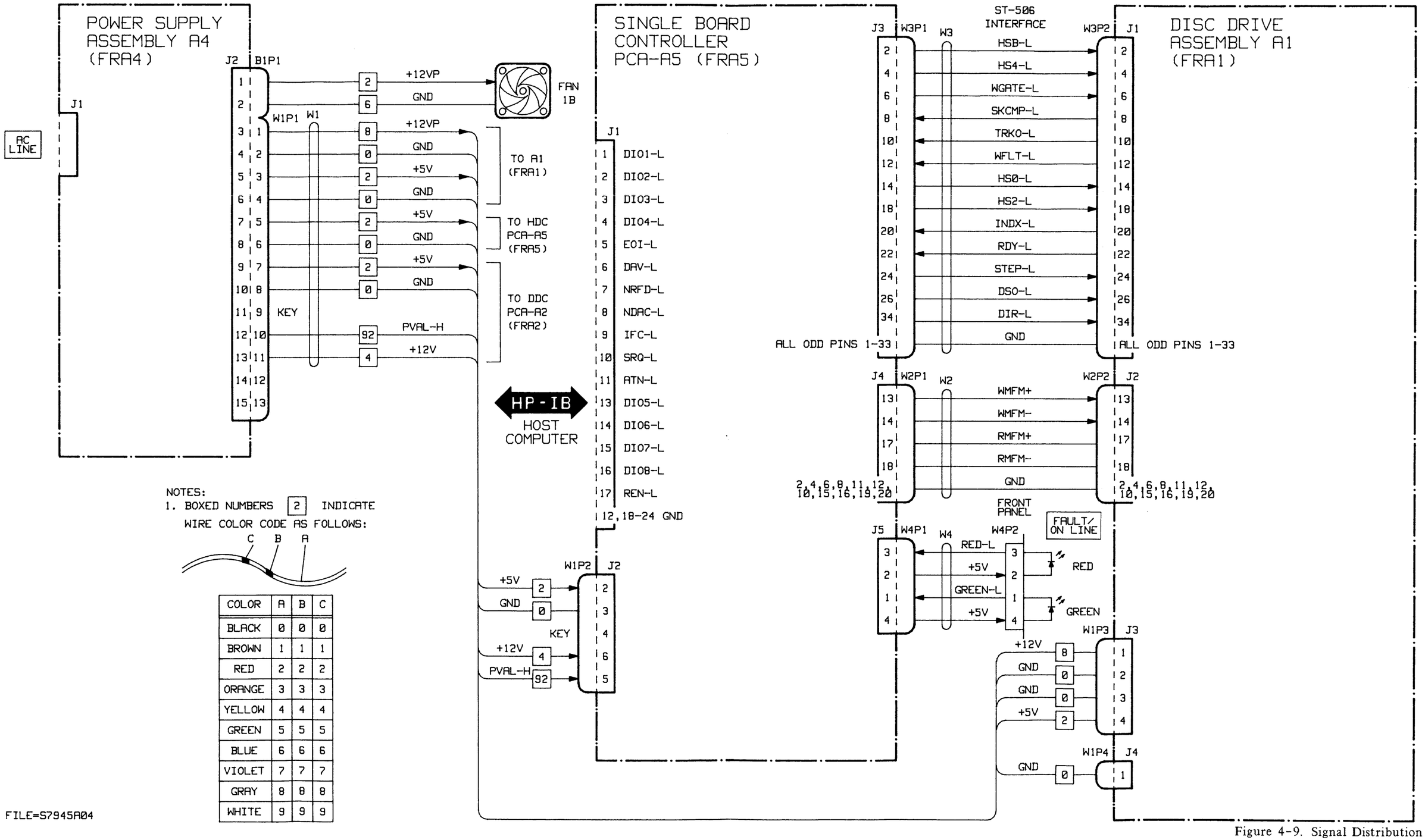


Figure 4-8. Cabling Diagram



NOTES:
1. BOXED NUMBERS [2] INDICATE WIRE COLOR CODE AS FOLLOWS:

COLOR	A	B	C
BLACK	0	0	0
BROWN	1	1	1
RED	2	2	2
ORANGE	3	3	3
YELLOW	4	4	4
GREEN	5	5	5
BLUE	6	6	6
VIOLET	7	7	7
GRAY	8	8	8
WHITE	9	9	9

FILE=S7945A04

Figure 4-9. Signal Distribution

5-1. INTRODUCTION

WARNING

The disc drive does not contain operator serviceable parts. To prevent electrical shock, refer all service activities to service-trained personnel.

CAUTION

- The field replaceable assemblies (FRA's) in the disc drive are electrostatic-sensitive devices. Take appropriate precautions when removing the FRA's from the disc drive. Use of an anti-static pad and wrist strap is required. (These components are contained in anti-static work station, part no. 9300-0749.) Immediately after removal, store the FRA's in anti-static, conductive plastic bags.

- The disc drive is delicate and should be handled with care. Also, the disc drive is heavier (9.9 kilograms/21.8 pounds) than its size would indicate.

- Do not turn the LINE~ switch on or off when the system is transferring data on the Hewlett-Packard Interface Bus (HP-IB).

- Do not cycle the LINE~ switch on and off unnecessarily.

- Do not connect or disconnect the HP-IB cable assembly(s) from the disc drive when the system is transferring data on the HP-IB.

This section provides removal and replacement procedures for field replaceable assemblies (FRA's) and parts in the disc drive. Procedures are given in the order in which disassembly normally occurs. Each part or assembly which must be removed before access can be gained to another assembly or part is presented first, followed by the next assembly which can be removed. This disassembly order is shown in figure 5-1. The locations of the FRA's are shown in figure 4-3. Figures 4-4 through 4-6 identify the connectors on the FRA's and their mating cable assembly connectors. Figure 4-8 provides an overall cabling diagram of the disc drive. References are also made to figure 6-1, Disc Drive, Exploded View, to assist in identifying and locating parts.

Note: TORX* hardware is used in the disc drive. This hardware requires the use of special drivers. In this manual, any reference to this type of hardware will be accompanied by the required driver size (for example, "T15").

5-2. PREPARATION FOR SERVICE

Before starting any removal or replacement procedure, prepare the disc drive for service as follows:

a. Set the disc drive LINE~ switch to the 0 (out) position and disconnect the power cord from the ~AC LINE connector.

b. Disconnect the HP-IB cable assembly from the disc drive HP-IB connector.

c. Place the disc drive on the anti-static pad and connect the wrist strap to the pad. When the top

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shroud is removed, (paragraph 5-4), ground the frame of the disc drive to the pad.

CAUTION

Ensure that the anti-static wrist strap is attached to the wrist before removing or replacing any components in the disc drive.

5-3. REMOVAL AND REPLACEMENT

Removal and replacement instructions for field replaceable assemblies (FRA's) and parts in the disc drive are provided in the following paragraphs. Unless otherwise specified, replacement is a reversal of the removal instructions.

5-4. TOP SHROUD

To remove the top shroud (1, figure 6-1), proceed as follows:

a. Perform the preparation for service procedure outlined in paragraph 5-2.

b. Ensure that the power cord is disconnected from the ~AC LINE connector on the rear panel of the disc drive.

c. Remove the three T10 screws (2, figure 6-1) which secure the top shroud to the disc drive.

d. Raise the rear of the top shroud upwards slightly and then move it backwards and away from the disc drive.

e. Ground the frame of the disc drive to the anti-static pad.

Reinstallation is a reversal of the removal procedure.

5-5. ROM Removal

To remove the EXEC ROM (3, figure 6-1) and/or the DDC ROM (4), proceed as follows:

a. Perform the preparation for service procedure outlined in outlined in paragraph 5-2. Pay particular attention to the instructions given for use of the anti-static pad and wrist strap.

b. Ensure that the power cord is disconnected from the ~AC LINE connector on the rear panel of the disc drive.

c. Remove the top shroud (refer to paragraph 5-4).

d. Remove the EXEC ROM (3) from the 28-pin socket on FRA5 (5). See figure 4-6 for the location of U178. Place the ROM on a piece of anti-static foam.

e. Remove the single DDC (4) from 28-pin socket on FRA5 (5). See figure 4-6 for the location of U176. Place the ROM on a piece of anti-static foam.

Reinstallation is a reversal of the removal procedure. The EXEC ROM is labeled U178 and the DDC ROM is labeled U176. Ensure that the EPROMS are installed in their matching 28-pin sockets on FRA5 (5), with the index notches on the ROM's facing toward the edge of FRA5. See figure 4-6.

5-6. FRA5 (SINGLE BOARD CONTROLLER PCA-A5)

To remove FRA5 (5, figure 6-1) from the disc drive, proceed as follows:

a. Perform the preparation for service procedure outlined in paragraph 5-2.

b. Ensure that the power cord is disconnected from the ~AC LINE connector on the rear panel of the disc drive.

c. Remove the top shroud (refer to paragraph 5-4).

d. Remove the two 6-32 hex standoffs (6) and lock washers (7) which secure the HP-IB connector on FRA5 (5) to the rear panel of the disc drive.

e. Disconnect connector P2 on power cable assembly W1 (22) from connector J2 on FRA5 (5)

f. Disconnect connectors W2P1 (8) and W3P1 (9) on the ribbon cable assemblies from connectors J3 and J4, respectively, on FRA5 (5).

g. Disconnect connector P1 on LED Cable Assembly W4 (12) from connector J5 on FRA5.

h. Slide FRA5 (5) forward and out of the disc drive.

Reinstallation is a reversal of the removal procedure. Before installing FRA5 in the disc drive, ensure that switch SW212 in FRA5 is set as follows. Refer to figure 4-6 for the location of SW212.

```
HP 7945: 1 - open (up)
         2 - closed (down)
         3 - open (up)
         4 - closed (down)

HP 7941: 1 - open (up)
         2 - closed (down)
         3 - closed (down)
         4 - closed (down)
```

Install the ROM kits (3, 4) as described in paragraph 5-5. Ensure also that the cable assembly connectors disconnected in steps e and f are firmly seated in their mating connectors.

5-7. FRONT PANEL

To remove the front panel (17, figure 6-1) from the disc drive, proceed as follows:

a. Perform the preparation for service procedure outlined in paragraph 5-2.

b. Ensure that the power cord is disconnected from the ~AC LINE connector on the rear panel of the disc drive.

c. Remove the top shroud (refer to paragraph 5-4).

d. Remove the four T10 screws (10) which secure the front shield (16), with front panel (17) and LED cable assembly W4 (12) attached, to the disc drive. Move the front panel forward away from the disc drive.

e. Disconnect connector P1 on LED cable assembly W4 (12) from connector J5 on FRA5 (5) and remove the front panel (17) from the disc drive.

f. If it is necessary to remove the front panel shield (16) from the front panel (17), proceed as follows:

(1) Remove the clip (11) which secures cable assembly W4 (12) to the front panel shield (16).

(2) Remove the four T25 screws (15) which secure the front panel shield (16) to the front panel (17).

(3) Remove the front panel shield (16) from the front panel (17).

Reinstallation is a reversal of the removal procedure. Ensure that the cable assembly connector disconnected in step e is properly seated in its mating connector. Check also that the LINE~ switch operates freely before tightening the four T10 screws (10) removed in step d.

5-8. FAN

To remove the fan (18, figure 6-1) from the disc drive, proceed as follows:

a. Perform the preparation for service procedure outlined in paragraph 5-2.

b. Ensure that the power cord is disconnected from the ~AC LINE connector on the rear panel of the disc drive.

c. Remove the top shroud (refer to paragraph 5-4), FRA5 (refer to paragraph 5-6), and the front panel (refer to paragraph 5-7).

d. Remove the four T20 screws (19) and grille (20), which secure the fan (18) to the rear panel.

Note: In early production runs of the disc drive, the fan attaching parts consist of four T15 machine screws and captive nuts. (See figure 6-1 in Appendix A or Appendix B.)

e. Disconnect the fan (18) power cable connector B1P1 from connector J2 on FRA4 (26).

f. Disengage the fan cable assembly from the two cable clamps (36) and remove the fan from the disc drive.

Reinstallation is a reversal of the removal procedure. Ensure that the fan is positioned with its power cable assembly in line with the cable clamps

(36). Ensure also that the cable assembly connector disconnected in step e is firmly seated in its mating connector. Before returning the disc drive to service, check that the fan is operating correctly.

5-9. FRA4 (POWER SUPPLY ASSEMBLY A4)

To remove FRA4 (26) from the disc drive, proceed as follows:

a. Perform the preparation for service procedure outlined in paragraph 5-2.

b. Ensure that the power cord is disconnected from the ~AC LINE connector on the rear panel of the disc drive.

c. Remove the top shroud (refer to paragraph 5-4) and the front panel (refer to paragraph 5-7).

d. Disconnect connector P1 on power cable assembly W1 (22) from connector J2 on FRA4 (26).

e. Disconnect the fan (18) cable assembly connector B1P1 from connector J2 on FRA4 (26).

f. Remove the T10 screw (23) and spacer (24) which secure FRA4 (26) to the mainframe assembly (37).

g. Remove the two T15 screws (25) which secure FRA4 (26) to the mainframe assembly (37).

h. Slide FRA4 (26) forward and out of the disc drive.

Reinstallation is a reversal of the removal procedure. Check that the cable assembly connectors disconnected in steps d and e are properly seated in their mating connector. Ensure that the T10 screw (23), and spacer (24) removed in step f are properly installed. Ensure also that the two T15 screws (25) removed in step g are properly replaced. This attaching hardware is required to properly ground the power supply to the mainframe assembly of the disc drive.

5-10. FRA1 (DISC DRIVE ASSEMBLY A1)

To remove FRA1 (33, figure 6-1) from the disc drive, proceed as follows.

Note: Before removing FRA1, refer to paragraph 4-47. This describes how to use a substitute FRA1 to verify the operation of FRA1 without removing it from the disc drive.

a. Perform the preparation for service procedure outlined in paragraph 5-2.

b. Ensure that the power cord is disconnected from the ~AC LINE connector on the rear panel of the disc drive.

c. Remove the top shroud (refer to paragraph 5-4) and the front panel (refer to paragraph 5-7).

d. Disconnect W2P2 (8) and W3P2 (9) ribbon cable assemblies from connecting J1 and J2, respectively on FRA1 (33).

e. Disconnect connectors P3 and P4 on power cable assembly W1 (22) from connectors J3 and J4, respectively, on FRA1 (33).

f. Remove the three T15 screws (34) which secure FRA1 (33) to the mainframe assembly (37).

g. Remove the T10 screw (35) which secures FRA1 (33) to the mainframe assembly (37).

h. Carefully withdraw FRA1 (33) from the mainframe assembly (37).

Reinstallation is a reversal of the removal process. Ensure that the cable assembly connectors disconnected in steps d and e are firmly seated in their mating connectors.

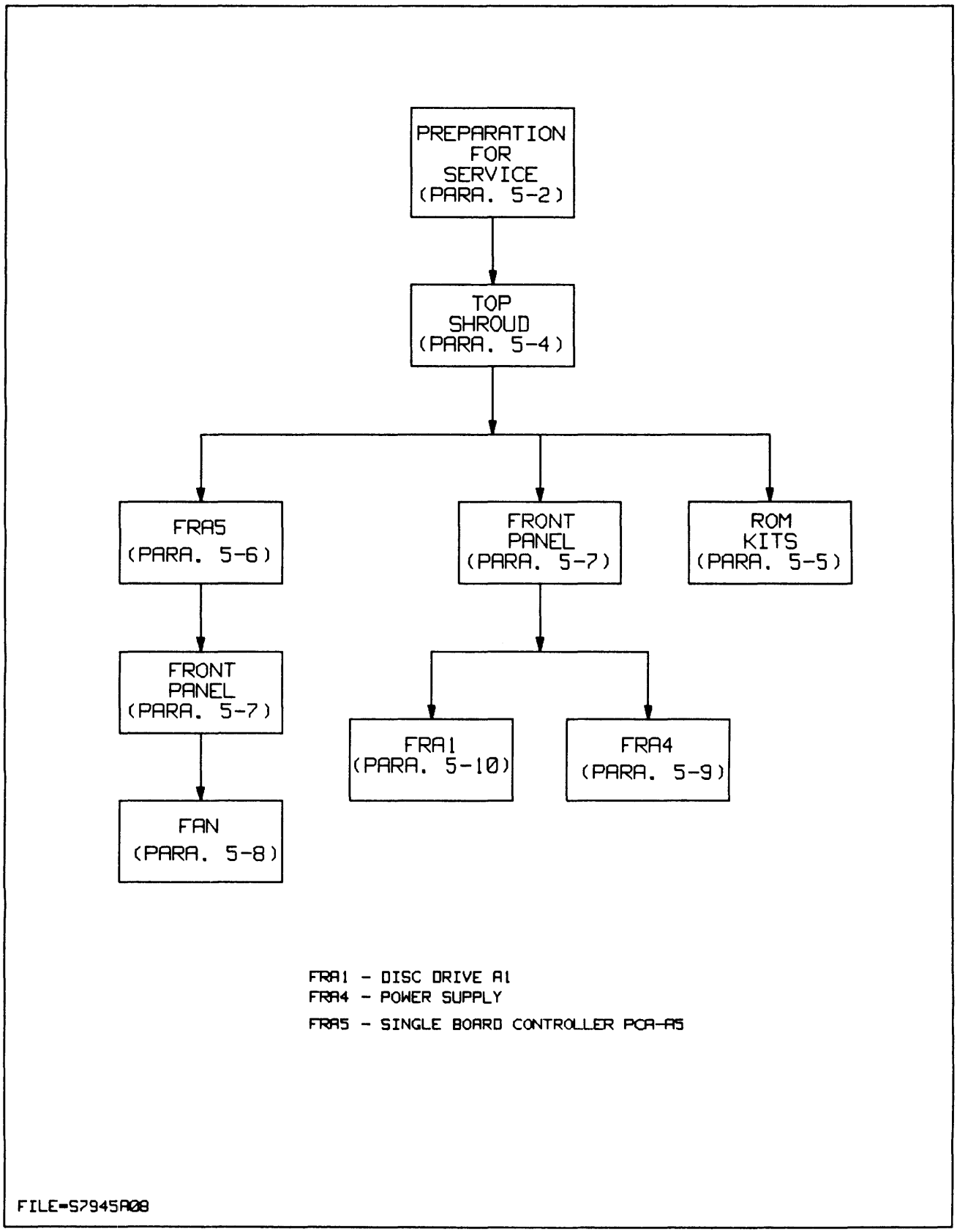

Figure 5-1. Order of Disassembly

REPLACEABLE PARTS

SECTION VI

6-1. INTRODUCTION

This section provides listings of all field-replaceable parts and an illustrated parts breakdown for the disc drive. Replaceable parts ordering information for the disc drive is also provided in this section.

Replaceable parts for the disc drive are listed in order of disassembly in table 6-1 and illustrated in figure 6-1. In each listing, attaching parts are listed immediately after the item they attach. Items in the DESCRIPTION column are indented to indicate their relationship to the next higher assembly. In addition, the symbol "---x---" follows the last attaching part for the item. Identification of the items and the labels is as follows:

Major Assembly

*Replaceable Assembly

*Attaching Part for Replacement Assembly

**Subassembly or Component Part

**Attaching Part for Subassembly or Replacement Part

The replaceable parts listings provide the following information for each part:

a. FIG & INDEX NO. The figure and index number which indicates where the replaceable part is illustrated.

b. HP PART NO. The Hewlett-Packard number for the replaceable part.

c. DESCRIPTION. The description of the replaceable part.

Refer to table 6-2 for an explanation of the abbreviations used in the DESCRIPTION column.

d. MFR CODE. The 5-digit code that denotes a typical manufacturer of a part. Refer to table 6-3 for a listing of manufacturers that correspond to the codes.

e. MFR PART NO. The manufacturer's part number for each replaceable part.

f. UNITS PER ASSEMBLY. The total quantity of each part used in the major assembly.

g. The MFR CODE and MFR PART NO. for common hardware are listed as 00000 and OBD (order by description), respectively, because these items can usually be purchased locally.

Note: TORX* hardware is used in the disc drive. This hardware requires the use of special drivers. In this manual, any reference to this type of hardware will be accompanied by the required driver size (for example, "T15").

6-2. ORDERING INFORMATION

To order replaceable parts for the disc drive, address the order to your local Hewlett-Packard Sales and Support Office. Sales and Support Offices are listed at the back of this manual. Specify the following information for each order:

a. Model and full serial number.

b. Hewlett-Packard part number.

c. Complete description of each part as provided in the replaceable parts listing.

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Table 6-1. Disc Drive Replaceable Parts

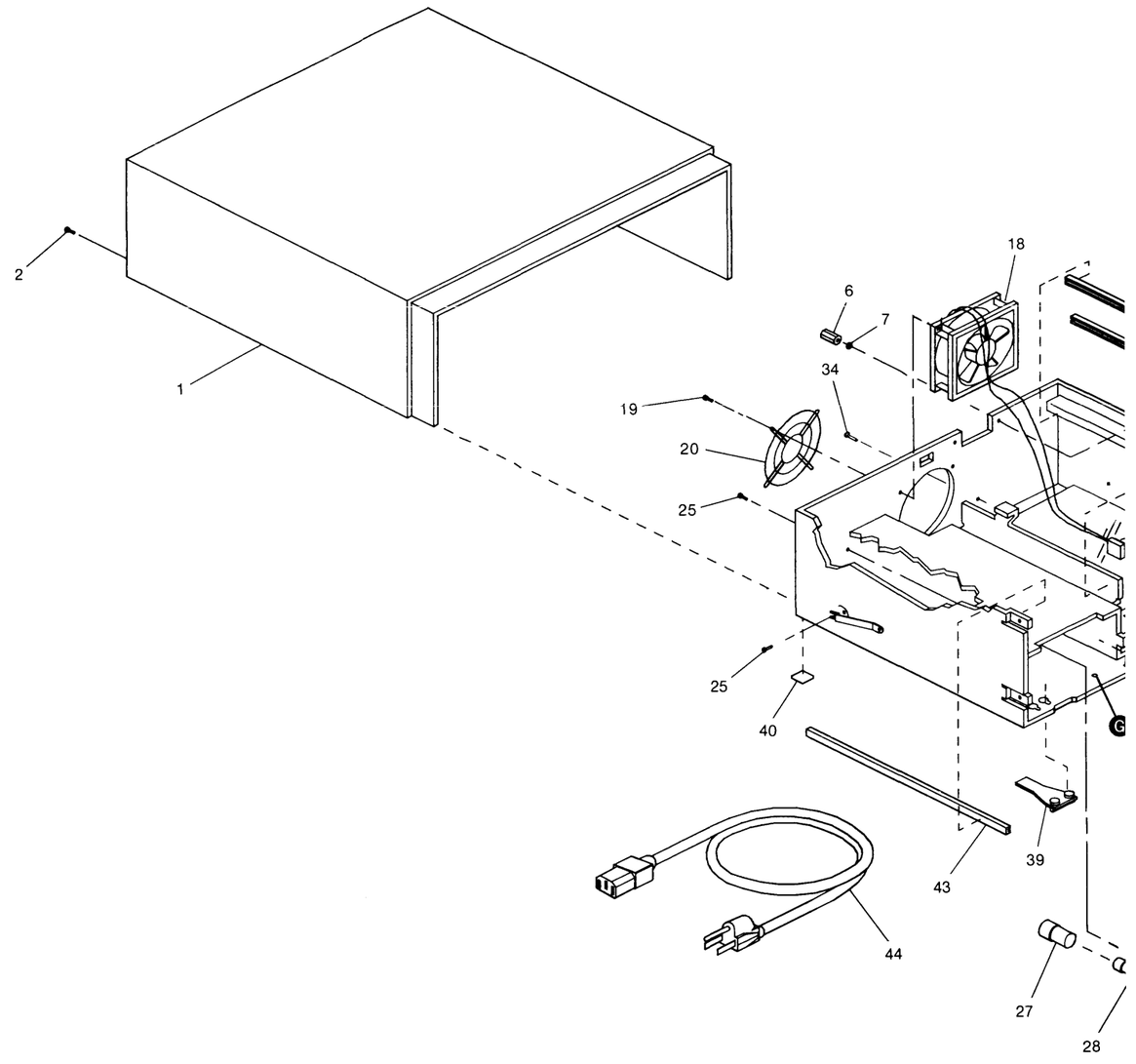
FIG.& INDEX NO.	HP PART NO.	DESCRIPTION	MFR CODE	MFR PART NO.	UNITS PER ASSY
6-1-	7941A	DISC DRIVE	28480	7941A	REF
	7945A	DISC DRIVE	28480	7945A	REF
1	07940-60028	*TOP SHROUD ASSEMBLY	28480	07940-60028	1
		(Attaching Parts)			
2	0515-0372	*SCREW, machine, pnh, T10, M3.0 by 0.5, 8 mm long, w/scw	00000	OBD	3
		- - - X - - -			
3	07941-10301	*ROM, EXEC	28480	07941-10301	1
4	07941-10401	*ROM DDC	28480	07941-10401	1
5	07941-60020	*SINGLE BOARD CONTROLLER PCA (A5-FRA5) Index items 3 and 4 are shipped with exchange assembly 07941-69020	28480	07941-60020	1
		(Attaching Parts)			
6	0380-0643	*STANDOFF, hex, 6-32, 0.255 in. long	28480	0380-0643	2
7	2190-0017	*WASHER, lock, helical, no. 8	00000	OBD	2
		- - - X - - -			
8	07941-60034	*CABLE ASSEMBLY (W2) (Data)	28480	07941-60034	1
9	07941-60036	*CABLE ASSEMBLY (W3) (Control)	28480	07941-60036	1
10	0515-0372	*SCREW, machine, pnh, T10, M3.0 by 0.5, 8 mm long, w/scw	00000	OBD	4
11	07940-00068	*CLIP	28480	07940-00068	1
12	07941-60033	*CABLE ASSEMBLY (W4)	28480	07941-60033	1
13	1990-0929	**LED, red	28480	1990-0929	1
14	1990-0930	**LED, green	28480	1990-0930	1
15	0624-0590	*SCREW, tapping, pnh, T25, 8-16, 0.312 in. long	00000	OBD	4
16	07940-60026	*SHIELD, front panel	28480	07940-60026	1
17	07941-60010	*FRONT PANEL ASSEMBLY, 7941	28480	07941-60010	1
	07945-60010	*FRONT PANEL ASSEMBLY, 7945	28480	07945-60010	REF
18	07941-60019	*FAN	28480	07941-60019	1
		(Attaching Parts)			
19	0624-0661	**SCREW, tapping, pnh, T20, 10-14, 0.625 in. long	00000	OBD	4
20	07941-00026	*GRILLE, fan	28480	07941-00026	1
21		Not assigned			
		- - - X - - -			
22	07941-60035	*CABLE ASSEMBLY (W1) (Power)	28480	07941-60035	1
23	0515-0665	*SCREW, machine, pnh, T10, M3.0 by 0.5, 14 mm long, w/scw	00000	OBD	1
24	0380-1746	*SPACER	28480	0380-1746	1
25	0515-0433	*SCREW, machine, pnh, T15, M4.0 by 0.70, 8 mm long, w/scw	00000	OBD	2
26	07940-60094	*POWER SUPPLY ASSEMBLY (A4/FRA4)	28480	07940-60094	1
27	2110-0565	**FUSEHOLDER, cap	28480	2110-0565	1
28	2110-0003	**FUSE, 3A, 250V, nontime delay 0.250 in. Dia.,1.25 in. long	75915	2A250V3.0A	1
29	5041-1203	**CAP	28480	5041-1203	1
30	0380-1655	**HOLDER, shaft	28480	0380-1655	1
31	09133-40202	**SHAFT, switch	28480	09133-40202	1
32	09144-45404	**SHIELD, power supply	28480	09144-45404	1

Table 6-1. Disc Drive Replaceable Parts, (Continued)

FIG.& INDEX NO.	HP PART NO.	DESCRIPTION	MFR CODE	MFR PART NO.	UNITS PER ASSY
33	07941-60021	*DISC DRIVE ASSEMBLY, 7941 (A1/FRA1)	28480	07941-60021	1
	07945-60021	*DISC DRIVE ASSEMBLY, 7945 (A1/FRA1) (Attaching Parts)	28480	07945-60021	REF
34	0515-0433	*SCREW, machine, pnh, T15, M4.0 by 0.70, 8 mm long, w/scw	00000	OBD	3
35	0515-0372	*SCREW, machine, pnh, T10, M3.0 by 0.50, 8 mm long, w/scw - - - X - - -	00000	OBD	1
36	1400-0510	*CLAMP, cable	02768	8511-28-00-9901	2
37	07941-60074	*MAINFRAME ASSEMBLY	28480	07941-60074	1
38	8160-0280	**CONTACT, finger	28480	8160-0280	1
39	09121-48303	**FOOT, front	28480	09121-48303	2
40	0403-0427	**FOOT, rear	94959	SJ-5008	2
41	0403-0268	**GUIDE, PCA, 5 in. long	28480	0403-0268	2
42	0403-0302	**GUIDE, PCA, 8 in. long	28480	0403-0302	2
43	0403-0379	**GUIDE, PCA, 9.9 in. long	28480	0403-0379	2
44	8120-1378	*POWER CORD ASSEMBLY, NEMA5A/CEE	28480	8120-1378	1
	8120-1351	*POWER CORD ASSEMBLY, BS 1363/CEE	28480	8120-1351	REF
	8120-1369	*POWER CORD ASSEMBLY, ASC 112/CEE	28480	8120-1369	REF
	8120-1689	*POWER CORD ASSEMBLY, GMBH/CEE	28480	8120-1689	REF
	8120-1860	*POWER CORD ASSEMBLY, CEE/CEE	28480	8120-1860	REF
	8120-2104	*POWER CORD ASSEMBLY, SEV/CEE	28480	8120-2104	REF
	8120-2956	*POWER CORD ASSEMBLY, MDPP/CEE	28480	8120-2956	REF
	8120-4211	*POWER CORD ASSEMBLY, SABS/CEE	28480	8120-4211	REF
45	8120-3445	*HP-IB CABLE ASSEMBLY, 1m, (Model 10833A)	28480	8120-3445	1

Table 6-1. Disc Drive Replaceable Parts, (Continued)

DESCRIPTION	MFR CODE	MFR PART NO.	UNITS PER ASSY
*DISC DRIVE ASSEMBLY, 7941 (A1/FRA1)	28480	07941-60021	1
*DISC DRIVE ASSEMBLY, 7945 (A1/FRA1)	28480	07945-60021	REF
(Attaching Parts)			
*SCREW, machine, pnh, T15, M4.0 by 0.70, 8 mm long, w/scw	00000	OBD	3
*SCREW, machine, pnh, T10, M3.0 by 0.50, 8 mm long, w/scw	00000	OBD	1
- - - X - - -			
*CLAMP, cable	02768	8511-28-00-9901	2
*MAINFRAME ASSEMBLY	28480	07941-60074	1
**CONTACT, finger	28480	8160-0280	1
**FOOT, front	28480	09121-48303	2
**FOOT, rear	94959	SJ-5008	2
**GUIDE, PCA, 5 in. long	28480	0403-0268	2
**GUIDE, PCA, 8 in. long	28480	0403-0302	2
**GUIDE, PCA, 9.9 in. long	28480	0403-0379	2
*POWER CORD ASSEMBLY, NEMA5A/CEE	28480	8120-1378	1
*POWER CORD ASSEMBLY, BS 1363/CEE	28480	8120-1351	REF
*POWER CORD ASSEMBLY, ASC 112/CEE	28480	8120-1369	REF
*POWER CORD ASSEMBLY, GMBH/CEE	28480	8120-1689	REF
*POWER CORD ASSEMBLY, CEE/CEE	28480	8120-1860	REF
*POWER CORD ASSEMBLY, SEV/CEE	28480	8120-2104	REF
*POWER CORD ASSEMBLY, MDPP/CEE	28480	8120-2956	REF
*POWER CORD ASSEMBLY, SABS/CEE	28480	8120-4211	REF
*HP-IB CABLE ASSEMBLY, 1m, (Model 10833A)	28480	8120-3445	1



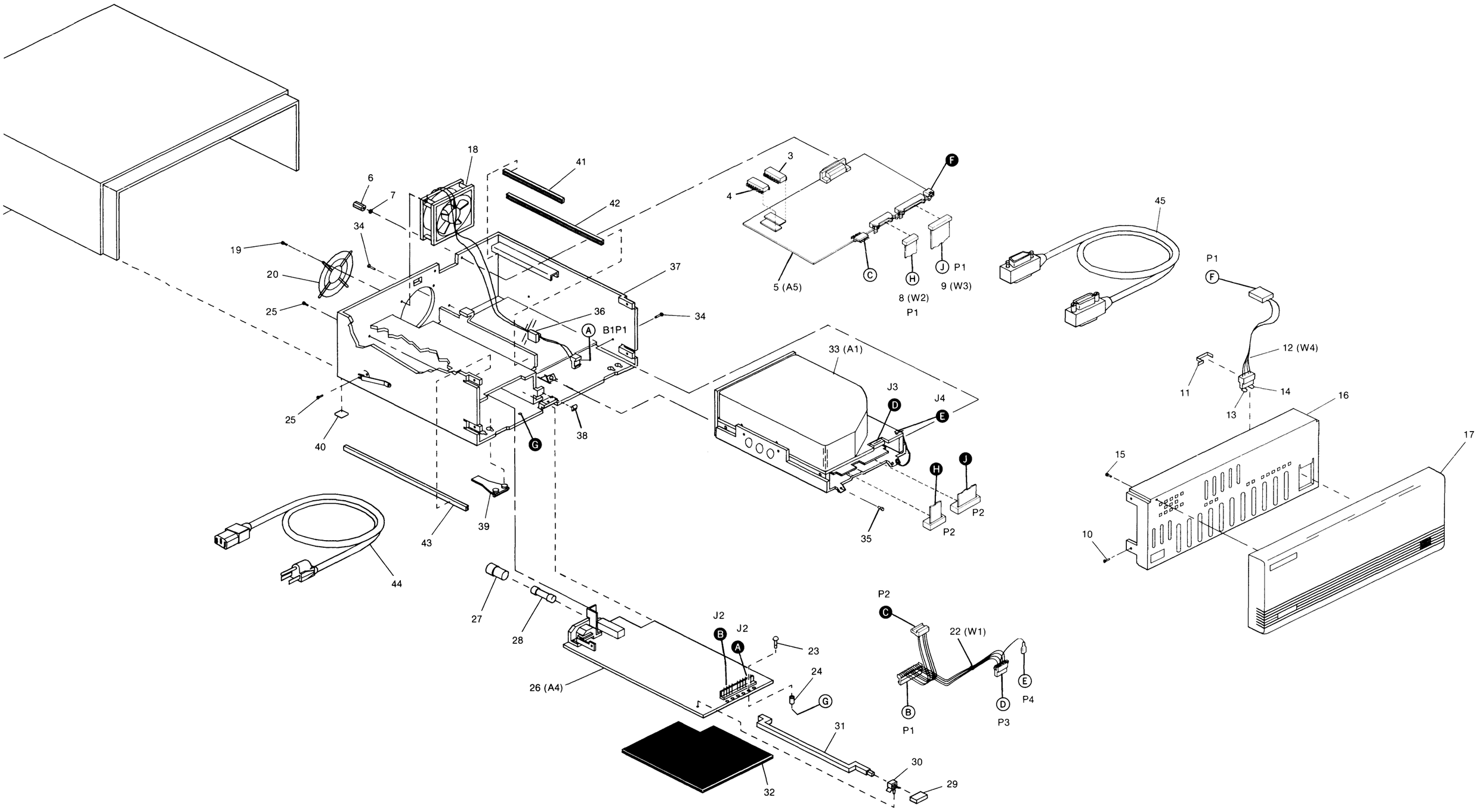


Figure 6-1. Disc Drive, Exploded View

Table 6-1. Disc Drive Replaceable Parts, (Continued)

FIG.& INDEX NO.	HP PART NO.	DESCRIPTION	MFR CODE	MFR PART NO.	UNITS PER ASSY
32	09133-40202	**SHAFT, switch	28480	09133-40202	1
33	09144-45404	**SHIELD, power supply	28480	09144-45404	1
34	0515-0433	*SCREW, machine, pnh, T15, M4.0 by 0.70, 8 mm long, w/scw	28480	00000 OBD	4
35	07941-00052	*BRACKET, mounting	28480	07941-00052	1
36	07941-20014	*SCREW, machine, pnh, T15, 6-32, 0.250 in. long, blue finish	28480	07941-20014	4
37	07941-60021	*DISC DRIVE ASSEMBLY, 7941 (A1/FRA1)	28480	07941-60021	1
	07945-60021	*DISC DRIVE ASSEMBLY, 7945 (A1/FRA1)	28480	07945-60021	REF
38	2360-0197	*SCREW, machine, pnh, pozi, 6-32, 0.375 in. long	00000	OBD	1
39	07941-60011	*GROUNDING STRAP	28480	07941-60011	1
40	2190-0321	*WASHER, lock, int tooth, no. 8	00000	OBD	1
41	1400-0510	*CLAMP, cable	02768	8511-28-00-9901	2
42	07941-60074	*MAINFRAME ASSEMBLY	28480	07941-60074	1
43	09121-48303	**FOOT, front	28480	09121-48303	2
44	0403-0427	**FOOT, rear	94959	SJ-5008	2
45	0403-0268	**GUIDE, PCA, 5 in. long	28480	0403-0268	2
46	0403-0302	**GUIDE, PCA, 8 in. long	28480	0403-0302	2
47	0403-0379	**GUIDE, PCA, 9.9 in. long	28480	0403-0379	2
48	8120-1378	*POWER CORD ASSEMBLY, NEMA5A/CEE	28480	8120-1378	1
	8120-1351	*POWER CORD ASSEMBLY, BS 1363/CEE	28480	8120-1351	REF
	8120-1369	*POWER CORD ASSEMBLY, ASC 112/CEE	28480	8120-1369	REF
	8120-1689	*POWER CORD ASSEMBLY, GMBH/CEE	28480	8120-1689	REF
	8120-1860	*POWER CORD ASSEMBLY, CEE/CEE	28480	8120-1860	REF
	8120-2104	*POWER CORD ASSEMBLY, SEV/CEE	28480	8120-2104	REF
	8120-2956	*POWER CORD ASSEMBLY, MDPP/CEE	28480	8120-2956	REF
49	8120-3445	*HP-IB CABLE ASSEMBLY, 1m, (Model 10833A)	28480	8120-3445	1

Table 6-3. Code List of Manufacturers

CODE NO.	MANUFACTURER	ADDRESS
02768	Illinois Tool Works, Inc.	Des Plaines, IL
28480	Hewlett-Packard Co.	Palo Alto, CA
75915	Tracor Littlefuse Inc.	Des Plaines, IL
94959	3M Co., Adhesives, Coatings, and Sealers Div.	St. Paul, MN

APPENDIX

SECTION
A

A-1. BACKDATING INFORMATION

This backdating appendix provides removal and replacement and replaceable parts information for HP 7941 and HP 7945 Disc Drives with serial numbers prefixed 2438 and prior. These disc drives utilize a removable mounting bracket for disc drive assembly A1/FRA1 and additional front panel attaching parts. Refer to Appendix B for theory of operation and service information for these disc drives.

CHANGE	DESCRIPTION
1	Sections V and VI in this backdating supplement should be used in place of Sections V and VI in the main manual for HP 7941 and HP 7945 Disc Drives with serial numbers prefixed 2438 and prior. Use Sections III and IV in Appendix B for theory of operation and service information for HP 7941 and HP 7945 Disc Drives with serial numbers prefixed 2438 and prior.

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5-1. INTRODUCTION

WARNING

The disc drive does not contain operator serviceable parts. To prevent electrical shock, refer all service activities to service-trained personnel.

CAUTION

- The field replaceable assemblies (FRA's) in the disc drive are electrostatic-sensitive devices. Take appropriate precautions when removing the FRA's from the disc drive. Use of an anti-static pad and wrist strap is required. (These components are contained in anti-static work station, part no. 9300-0749.) Immediately after removal, store the FRA's in anti-static, conductive plastic bags.

- The disc drive is delicate and should be handled with care. Also, the disc drive is heavier (9.9 kilograms/21.8 pounds) than its size would indicate.

- Do not turn the LINE~ switch on or off when the system is transferring data on the Hewlett-Packard Interface Bus (HP-IB).

- Do not cycle the LINE~ switch on and off unnecessarily.

- Do not connect or disconnect the HP-IB cable assembly(s) from the disc drive when the system is transferring data on the HP-IB.

This section provides removal and replacement procedures for field replaceable assemblies (FRA's) and parts in the disc drive. Procedures are given in the order in which disassembly normally occurs. Each part or assembly which must be removed before access can be gained to another assembly or part is presented first, followed by the next assembly which can be removed. This disassembly order is shown in figure 5-1. The locations of the FRA's are shown in figure 4-3 in Appendix B . Figures 4-4 through 4-7 (in Appendix B) identify the connectors on the FRA's and their mating cable assembly connectors. Figure 4-9 (in Appendix B) provides an overall cabling diagram of the disc drive. References are also made to figure 6-1, Disc Drive, Exploded View, to assist in identifying and locating parts.

Note: TORX* hardware is used in the disc drive. This hardware requires the use of special drivers. In this manual, any reference to this type of hardware will be accompanied by the required driver size (for example, "T15").

5-2. PREPARATION FOR SERVICE

Before starting any removal or replacement procedure, prepare the disc drive for service as follows:

a. Set the disc drive LINE~ switch to the 0 (out) position and disconnect the power cord from the ~AC LINE connector.

b. Disconnect the HP-IB cable assembly from the disc drive HP-IB connector.

c. Place the disc drive on the anti-static pad and connect the wrist strap to the pad. When the top shroud is removed, (paragraph 5-4), ground the frame of the disc drive to the pad.

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CAUTION

Ensure that the anti-static wrist strap is attached to the wrist before removing or replacing any components in the disc drive.

5-3. REMOVAL AND REPLACEMENT

Removal and replacement instructions for field replaceable assemblies (FRA's) and parts in the disc drive are provided in the following paragraphs. Unless otherwise specified, replacement is a reversal of the removal instructions.

5-4. TOP SHROUD

To remove the top shroud (1, figure 6-1), proceed as follows:

a. Perform the preparation for service procedure outlined in paragraph 5-2.

b. Ensure that the power cord is disconnected from the ~AC LINE connector on the rear panel of the disc drive.

c. Remove the three T10 screws (2, figure 6-1) which secure the top shroud to the disc drive.

d. Raise the rear of the top shroud upwards slightly and then move it backwards and away from the disc drive.

e. Ground the frame of the disc drive to the anti-static pad.

Reinstallation is a reversal of the removal procedure.

5-5. EPROM KITS

To remove the EXEC EPROM kit (3, figure 6-1) and/or the DISC EPROM kit (4), proceed as follows:

a. Perform the preparation for service procedure outlined in outlined in paragraph 5-2. Pay particular attention to the instructions given for use of the anti-static pad and wrist strap.

b. Ensure that the power cord is disconnected from the ~AC LINE connector on the rear panel of the disc drive.

c. Remove the top shroud (refer to paragraph 5-4).

d. Remove the single EXEC EPROM (3) from the 28-pin socket U101 on FRA5 (5). See figure 4-7 (in Appendix B) for the location of U101. Place the EPROM on a piece of anti-static foam.

e. Remove the two DISC EPROM's (4) from 28-pin sockets U131 and U161 on FRA5 (5). See figure 4-7 (in Appendix B). Place the EPROM's on a piece of anti-static foam.

Reinstallation is a reversal of the removal procedure. The EXEC EPROM is labeled U101 and the DISC EPROM's are labeled U131 and U161. Ensure that the EPROMS are installed in their matching 28-pin sockets on FRA5 (5), with the index notches on the EPROM's facing toward the edge of FRA5. See figure 4-7.

5-6. FRA5 (HOST DEPENDENT CONTROLLER PCA-A5)

To remove FRA5 (5, figure 6-1) from the disc drive, proceed as follows:

a. Perform the preparation for service procedure outlined in paragraph 5-2.

b. Ensure that the power cord is disconnected from the ~AC LINE connector on the rear panel of the disc drive.

c. Remove the top shroud (refer to paragraph 5-4).

d. Remove the two 6-32 hex standoffs (6) and lock washers (7) which secure the HP-IB connector on FRA5 (5) to the rear panel of the disc drive.

e. Disconnect connector P2 on power cable assembly W1 (23) from connector J4 on FRA5 (5)

f. Disconnect connector P1 on ribbon cable assembly W2 (22) from connector J2 on FRA5 (5)

g. Slide FRA5 (5) forward and out of the disc drive.

Reinstallation is a reversal of the removal procedure. Before installing FRA5, ensure that there is a circuit board jumper (5A) in place on the two "DISK OR TAPE" pins at W2 on FRA5. Ensure also that there is a circuit board jumper (5A) in place on the two pins at W1. See figure 4-7 in Appendix B for the locations of W1 and W2.

Install the EPROM kits (3, 4) as described in paragraph 5-5. Ensure also that the cable assembly connectors disconnected in steps e and f are firmly seated in their mating connectors.

5-7. FRONT PANEL

To remove the front panel (15, figure 6-1) from the disc drive, proceed as follows:

a. Perform the preparation for service procedure outlined in paragraph 5-2.

b. Ensure that the power cord is disconnected from the ~AC LINE connector on the rear panel of the disc drive.

c. Remove the top shroud (refer to paragraph 5-4).

d. Place the disc drive on its side and remove the T10 screw (8) which secures shield (14), with front panel (15) and cable assembly (10) attached, to the disc drive. See figure 6-1, detail A.

e. Return the disc drive to an upright position. Remove the remaining four T10 screws (8) which secure the front shield (14), with front panel (15) and LED cable assembly W4 (10) attached, to the disc drive. Move the front panel forward away from the disc drive.

f. Disconnect connector P1 on LED cable assembly W4 (10) from connector J5 on FRA2 (21) and remove the front panel (15) from the disc drive.

g. If it is necessary to remove the front panel shield (14) from the front panel (15), proceed as follows:

(1) Remove the clip (9) which secures cable assembly W4 (10) to the front panel shield (14).

(2) Remove the four T25 screws (13) which secure the front panel shield (14) to the front panel (15).

(3) Remove the front panel shield (14) from the front panel (15).

Reinstallation is a reversal of the removal procedure. Ensure that the cable assembly connector disconnected in step f is properly seated in its mating connector. Check also that the LINE~ switch operates freely before tightening the five T10 screws (8) removed in steps d and e.

5-8. FAN

To remove the fan (16, figure 6-1) from the disc drive, proceed as follows:

a. Perform the preparation for service procedure outlined in paragraph 5-2.

b. Ensure that the power cord is disconnected from the ~AC LINE connector on the rear panel of the disc drive.

c. Remove the top shroud (refer to paragraph 5-4), FRA5 (refer to paragraph 5-6), and the front panel (refer to paragraph 5-7).

d. Remove the four T15 screws (17), grille (18), and nuts (19) which secure the fan (16) to the rear panel.

e. Disconnect the fan (16) power cable connector B1P1 from connector J2 on FRA4 (27).

f. Disengage the fan cable assembly from the two cable clamps (41) and remove the fan from the disc drive.

Reinstallation is a reversal of the removal procedure. Ensure that the fan is positioned with its power cable assembly in line with the cable clamps (41). Ensure also that the cable assembly connector disconnected in step e is firmly seated in its mating connector. Before returning the disc drive to service, check that the fan is operating correctly.

5-9. FRA2 (DDC PCA-A2)

To remove FRA2 (21) from the disc drive, proceed as follows:

a. Perform the preparation for service procedure outlined in paragraph 5-2.

b. Ensure that the power cord is disconnected from the ~AC LINE connector on the rear panel of the disc drive.

c. Remove the top shroud (refer to paragraph 5-4) and the front panel (refer to paragraph 5-7).

d. Disconnect connector P3 on power cable assembly W1 (23) from connector J1 on FRA2 (21).

e. Disconnect connectors P1 and P2 on ribbon cable assembly W3 (20) from connectors J3 and J4, respectively, on FRA2 (21).

f. Disconnect connector P1 on LED cable assembly W4 (10) from connector J5 on FRA2 (21).

g. Disconnect connector P1 on ribbon cable assembly W2 (22) from connector J2 on PCA-A5 (5).

h. Carefully slide FRA2 (21), with cable assembly W2 (22) attached, out of the disc drive.

i. Disconnect connector P2 on ribbon cable assembly W2 (22) from connector J2 on FRA2 (21) and remove the cable assembly.

Reinstallation is a reversal of the removal procedure. Before installing FRA2 in the disc drive, ensure that switch U484 in FRA2 is set as follows. Refer to figure 4-5 in Appendix B for the location of U484.

```
HP 7945: 1 - open (up)
         2 - closed (down)
         3 - open (up)
         4 - closed (down)

HP 7941: 1 - open (up)
         2 - closed (down)
         3 - closed (down)
         4 - closed (down)
```

Ensure also that the cable assembly connectors disconnected in steps d through g and step i are properly seated in their mating connectors.

5-10. FRA4 (POWER SUPPLY ASSEMBLY A4)

To remove FRA4 (27) from the disc drive, proceed as follows:

a. Perform the preparation for service procedure outlined in paragraph 5-2.

b. Ensure that the power cord is disconnected from the ~AC LINE connector on the rear panel of the disc drive.

c. Remove the top shroud (refer to paragraph 5-4) and the front panel (refer to paragraph 5-7).

d. Disconnect connector P1 on power cable assembly W1 (23) from connector J2 on FRA4 (27).

e. Disconnect the fan (16) cable assembly connector B1P1 from connector J2 on FRA4 (27).

f. Remove the T10 screw (24) and spacer (25) which secure FRA4 (27) to the mainframe assembly (42).

g. Remove the two T15 screws (26) which secure FRA4 (27) to the mainframe assembly (42).

h. Slide FRA4 (27) forward and out of the disc drive.

Reinstallation is a reversal of the removal procedure. Check that the cable assembly connectors disconnected in steps d and e are properly seated in their mating connector. Ensure that the T10 screw (24), and spacer (25) removed in step f are properly installed. Ensure also that the two T15 screws (26) removed in step g are properly replaced. This attaching hardware is required to properly ground the power supply to the mainframe assembly of the disc drive.

5-11. FRA1 (DISC DRIVE ASSEMBLY A1)

To remove FRA1 (37, figure 6-1) from the disc drive, proceed as follows.

Note: Before removing FRA1, refer to paragraph 4-47 in Appendix B. This describes how to use a substitute FRA1 to verify the operation of FRA1 without removing it from the disc drive.

a. Perform the preparation for service procedure outlined in paragraph 5-2.

b. Ensure that the power cord is disconnected from the ~AC LINE connector on the rear panel of the disc drive.

c. Remove the top shroud (refer to paragraph 5-4) and the front panel (refer to paragraph 5-7).

d. Disconnect connectors P3 and P4 on ribbon cable assembly W3 (20) from connectors J1 and J2, respectively, on FRA1 (37).

e. Disconnect connectors P4 and P5 on power cable assembly W1 (23) from connectors J3 and J4, respectively, on FRA1 (37).

f. Place the disc drive on its side and remove the T15 screw (34) which secures mounting bracket (35), with FRA1 (37) attached, to the bottom of the mainframe assembly (42). See figure 6-1, detail A.

g. Return the disc drive to an upright position. Remove the remaining three T15 screws (34) which secure mounting bracket (35) with FRA1 (37) attached, to disc drive.

h. Remove mounting bracket (35), with FRA1 (37) attached, from the disc drive.

i. Remove the four blue-colored T15 6-32 screws (36) which secure FRA1 (37) to the mounting bracket (35) and remove FRA1.

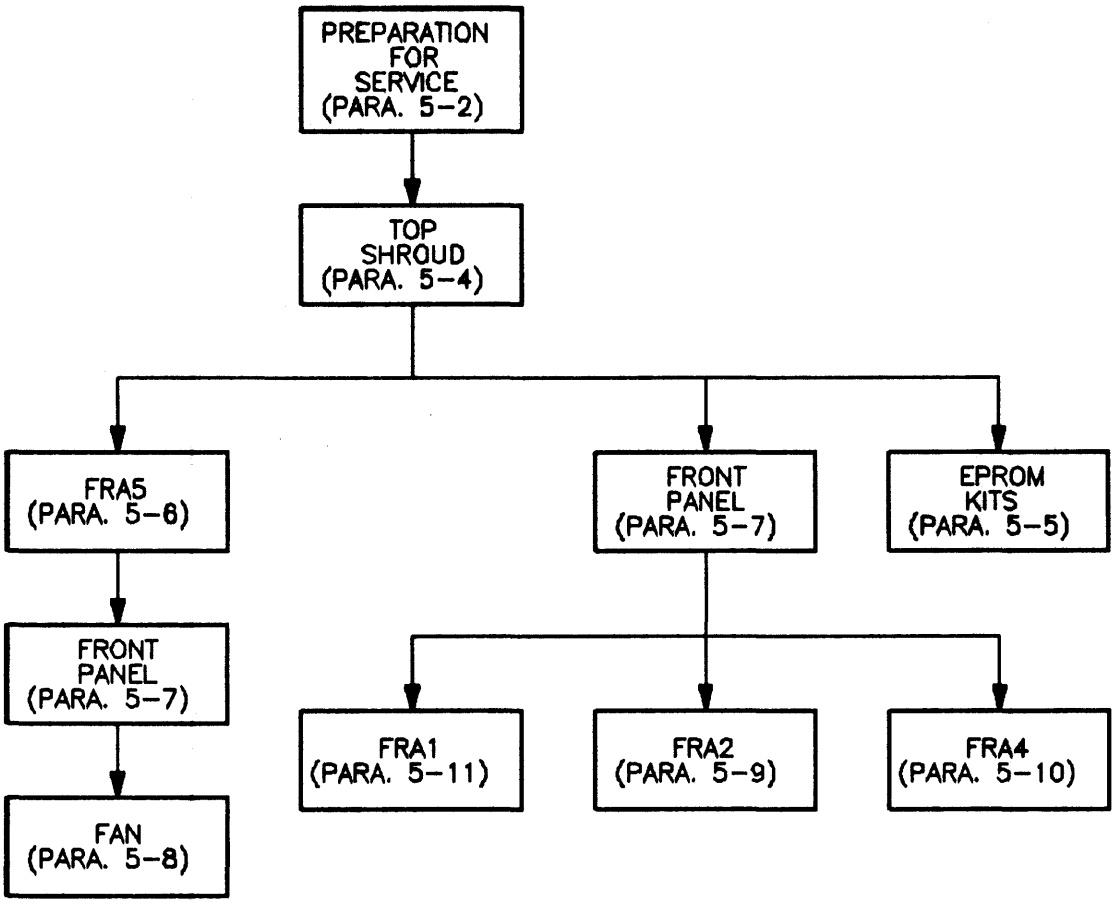
j. Remove the pozi 6-32 screw (38) which secures grounding strap (39) and lockwasher (40) to FRA1 (37) and remove the grounding strap.

CAUTION

Use only the four blue-colored T15 6-32 screws (36) removed in step i to attach mounting bracket (35) to FRA1 (37). Use of metric TORX* attaching screws will strip the 6-32 threads in FRA1.

Reinstallation is a reversal of the removal process. Ensure that the cable assembly connectors disconnected in steps d and e are firmly seated in their mating connectors. Ensure also that the grounding strap (39) removed in step j is properly attached between FRA1 and the mainframe assembly.

*TORX is a registered tradename of the Camcar Division of Textron, Inc.



FRA1 – DISC DRIVE A1

FRA2 – DEVICE DEPENDENT CONTROLLER PCA–A2

FRA4 – POWER SUPPLY A4

FRA5 – HOST DEPENDENT CONTROLLER PCA–A5

FILE=FSJEF17A

Figure 5-1. Order of Disassembly

REPLACEABLE PARTS

SECTION VI

6-1. INTRODUCTION

This section provides listings of all field-replaceable parts and an illustrated parts breakdown for the disc drive. Replaceable parts ordering information for the disc drive is also provided in this section.

Replaceable parts for the disc drive are listed in order of disassembly in table 6-1 and illustrated in figure 6-1. In each listing, attaching parts are listed immediately after the item they attach. Items in the DESCRIPTION column are indented to indicate their relationship to the next higher assembly. In addition, the symbol "---x---" follows the last attaching part for the item. Identification of the items and the labels is as follows:

Major Assembly

*Replaceable Assembly

*Attaching Part for Replacement Assembly

**Subassembly or Component Part

**Attaching Part for Subassembly or Replacement Part

The replaceable parts listings provide the following information for each part:

a. FIG & INDEX NO. The figure and index number which indicates where the replaceable part is illustrated.

b. HP PART NO. The Hewlett-Packard number for the replaceable part.

c. DESCRIPTION. The description of the replaceable part.

Refer to table 6-2 for an explanation of the abbreviations used in the DESCRIPTION column.

d. MFR CODE. The 5-digit code that denotes a typical manufacturer of a part. Refer to table 6-3 for a listing of manufacturers that correspond to the codes.

e. MFR PART NO. The manufacturer's part number for each replaceable part.

f. UNITS PER ASSEMBLY. The total quantity of each part used in the major assembly.

g. The MFR CODE and MFR PART NO. for common hardware are listed as 00000 and OBD (order by description), respectively, because these items can usually be purchased locally.

Note: TORX* hardware is used in the disc drive. This hardware requires the use of special drivers. In this manual, any reference to this type of hardware will be accompanied by the required driver size (for example, "T15").

6-2. ORDERING INFORMATION

To order replaceable parts for the disc drive, address the order to your local Hewlett-Packard Sales and Support Office. Sales and Support Offices are listed at the back of this manual. Specify the following information for each order:

a. Model and full serial number.

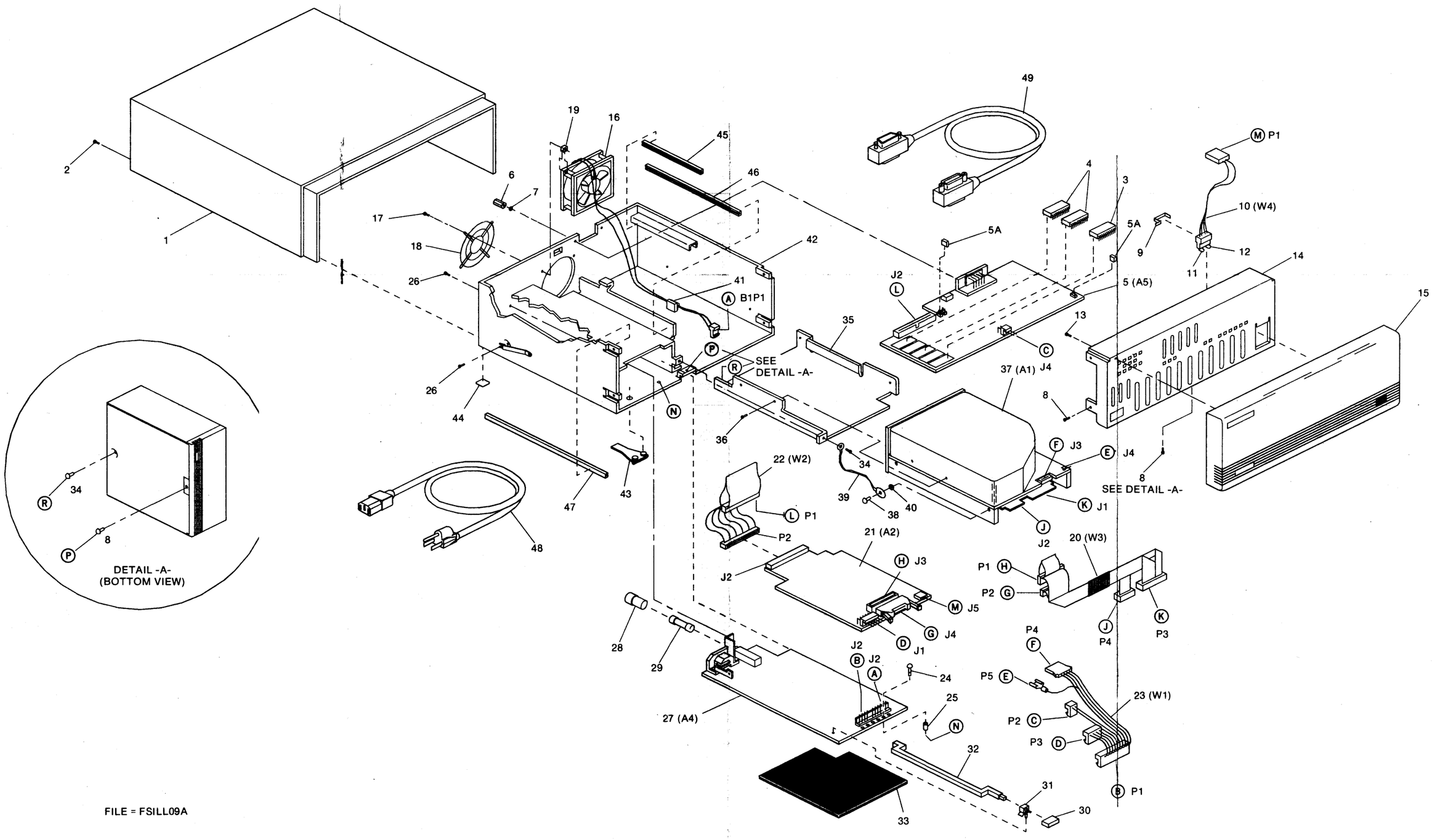
b. Hewlett-Packard part number.

c. Complete description of each part as provided in the replaceable parts listing.

*TORX is a registered trademark of the Camcar Division of Textron, Inc.

Table 6-1. Disc Drive Replaceable Parts

FIG.& INDEX NO.	HP PART NO.	DESCRIPTION	MFR CODE	MFR PART NO.	UNITS PER ASSY
6-1-	7941A	DISC DRIVE	28480	7941A	REF
	7945A	DISC DRIVE	28480	7945A	REF
1	07940-60028	*TOP SHROUD ASSEMBLY (Attaching Parts)	28480	07940-60028	1
2	0515-0372	*SCREW, machine, pnh, T10, M3.0 by 0.5, 8 mm long, w/scw - - - X - - -	00000	OBD	3
3	07940-10103	*EPROM KIT, EXEC	28480	07940-10103	1
4	07940-10202	*EPROM KIT, DISC	28480	07940-10202	1
5	07940-60195	*HOST DEPENDENT CONTROLLER PCA (A5/FRA5)	28480	07940-60195	1
5A	1285-0221	**JUMPER, circuit board (W1, W2/W3) (Attaching Parts)	28480	1285-0221	2
6	0380-0643	*STANDOFF, hex, 6-32, 0.255 in. long	28480	0380-0643	2
7	2190-0017	*WASHER, lock, helical, no. 8 - - - X - - -	00000	OBD	2
8	0515-0372	*SCREW, machine, pnh, T10, M3.0 by 0.5, 8 mm long, w/scw	00000	OBD	5
9	07940-00068	*CLIP	28480	07940-00068	1
10	07941-60033	*CABLE ASSEMBLY (W4)	28480	07941-60033	1
11	1990-0929	**LED, red	28480	1990-0929	1
12	1990-0930	**LED, green	28480	1990-0930	1
13	0624-0590	*SCREW, tapping, pnh, T25, 8-16, 0.312 in. long	00000	OBD	4
14	07940-60026	*SHIELD, front panel	28480	07940-60026	1
15	07941-60010	*FRONT PANEL ASSEMBLY, 7941	28480	07941-60010	1
	07945-60010	*FRONT PANEL ASSEMBLY, 7945	28480	07945-60010	REF
16	07941-60019	*FAN (Attaching Parts)	28480	07941-60019	1
17	2360-0469	*SCREW, machine, pnh, T15, 6-32 0.750 in. long, w/scw	00000	OBD	4
18	07941-00026	*GRILLE, fan	28480	07941-00026	1
19	0590-1245	*NUT, sheetmetal - - - X - - -	28480	0590-1245	4
20	07941-60008	*CABLE ASSEMBLY (W3)	28480	07941-60008	1
21	07941-60102	*DEVICE DEPENDENT CONTROLLER PCA (A2/FRA2)	28480	07941-60102	1
22	07941-60007	*CABLE ASSEMBLY (W2)	28480	07941-60007	1
23	07941-60009	*CABLE ASSEMBLY (W1)	28480	07941-60009	1
24	0515-0665	*SCREW, machine, pnh, T10, M3.0 by 0.5, 14 mm long, w/scw	00000	OBD	1
25	0380-1746	*SPACER	28480	0380-1746	1
26	0515-0433	*SCREW, machine, pnh, T15, M4.0 by 0.70, 8 mm long, w/scw	00000	OBD	2
27	07940-60094	*POWER SUPPLY ASSEMBLY (A4/FRA4)	28480	07940-60094	1
28	2110-0565	**FUSEHOLDER, cap	28480	2110-0565	1
29	2110-0003	**FUSE, 3A, 250V, nontime delay 0.250 in. Dia., 1.250 in. long	75915	2A250V3.0A	1
30	5041-1203	**CAP	28480	5041-1203	1
31	0380-1655	**HOLDER, shaft	28480	0380-1655	1



FILE = FSILL09A

Figure 6-1. Disc Drive, Exploded View

Table 6-2. Abbreviations

A	= ampere(s)	incand	= incandescent	qty	= quantity
ac	= alternating current	incl	= include(s)		
		intl	= internal	rdh	= round head
AR	= as required	I/O	= input/output	rect	= rectifier
assy	= assembly			ref	= reference
		k	= kilo (10^3), kilohm	rf	= radio frequency
brkt	= bracket			rfi	= radio frequency interference
		kg	= kilogram		
c	= centi (10^{-2})			rh	= right hand
C	= Celsius, centigrade	lb	= pound	rpm	= revolutions per minute
		LED	= light-emitting diode		
cer	= ceramic			rwv	= reverse working voltage
cm	= centimetre	lh	= left hand		
comp	= composition				
conn	= connector	M	= mega (10^6), megohm	sb	= slow blow
				SCR	= semiconductor-controlled rectifier
d	= deci (10^{-1})	m	= milli (10^{-3})		
dc	= direct current	mach	= machine		
deg	= degree(s)	mb	= medium blow	scw	= square cone washer
dia	= diameter	met oxd	= metal oxide		
dpdt	= double-pole, double-throw	mfr	= manufacturer	Se	= selenium
		misc	= miscellaneous	Si	= silicon
dpst	= double-pole, single throw	mm	= millimetre	slftpg	= self-tapping
		mtg	= mounting	spdt	= single-pole, double throw
		My	= Mylar		
elctlt	= electrolytic			spst	= single pole, single throw
encap	= encapsulated	n	= nano (10^{-9})		
ext	= external	n.c.	= normally closed	sst	= stainless steel
		no.	= number	stl	= steel
F	= Fahrenheit, farad	NSR	= not separately replaceable	sw	= switch
				T	= TORX(R) screw
fb	= fast blow	ntd	= no time delay	Ta	= tantalum
fh	= flat head			tgl	= toggle
fig.	= figure	OBD	= order by description	thd	= thread
filh	= fillister head			Ti	= titanium
flm	= film	OD	= outside diameter	tol	= tolerance
fw	= full wave				
fxd	= fixed	ovh	= oval head		
		oxd	= oxide	U (μ)	= micro (10^{-6})
G	= giga (10^9)				
Ge	= germanium	p	= pico (10^{-12})	V	= volt(s)
		PCA	= printed-circuit assembly	var	= variable
H	= Henry, Henries			Vdcw	= direct current working volts
hd	= head	phh	= phillips head		
hex	= hexagon, hexagonal	pnh	= pan head		
		P/O	= part of	W	= watt(s)
hlcl	= helical	pot	= potentiometer	w/	= with
Hz	= Hertz	pozi	= Pozidriv	WIV	= inverse working volts
ID	= inside diameter			ww	= wire-wound
in.	= inch, inches				

TORX(R) is a registered trademark of the Camcar Division of Textron, Inc. (abbrev-8/83)

Table 6-3. Code List of Manufacturers

CODE NO.	MANUFACTURER	ADDRESS
02768	Illinois Tool Works, Inc.	Des Plaines, IL
28480	Hewlett-Packard Co.	Palo Alto, CA
75915	Tracor Littlefuse Inc.	Des Plaines, IL
94959	3M Co., Adhesives, Coatings, and Sealers Div.	St. Paul, MN

APPENDIX

SECTION B

B-1. BACKDATING INFORMATION

This backdating appendix provides theory of operation, service information, removal and replacement, and replaceable parts information for HP 7941 and HP 7945 Disc Drives with serial numbers prefixed 2515 and prior. These disc drives have a dual controller configuration using a individual host dependent and device dependent controllers.

CHANGE	DESCRIPTION
1	Sections III and IV in this backdating supplement should be used in place of Sections III and IV in the main manual for HP 7941 and HP 7945 Disc Drives with serial numbers prefixed 2515 and prior. Sections V and VI in this backdating supplement should be used in place of Sections V and VI in the main manual for HP 7941 and HP 7945 Disc Drives with serial numbers prefixed from 2439 through 2515.

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SERVICE INFORMATION

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Appendix B

THEORY OF OPERATION

3-1. INTRODUCTION

The HP 7941 and HP 7945 Disc Drives are medium performance, random access, mass storage devices intended for use with small and medium sized computers. The formatted storage capacities of the HP 7941 and HP 7945 are 24 megabytes and 55 megabytes, respectively. In this section, "disc drive" refers to both the HP 7941 and 7945, unless otherwise specified.

The head-disc module in the disc drive is sealed and uses two (HP 7941) or four (HP 7945) 130-millimetre (5.12-inch) diameter nonremovable discs. One read/write head is used for each disc surface. The bottom surface of the lowest disc in the stack contains continuous prerecorded servo data which is used to ensure the precise positioning of the read/write heads.

The disc drive employs a peripheral mass storage control structure which consists of a host dependent controller (HDC) and a device dependent controller (DDC). See figure 3-3. In this structure, the common functions of typical mass storage devices (disc drive, tape drive) are consolidated in the HDC and drive dependent tasks are performed by the DDC. The common functions of the HDC include: host interface, direct memory access (DMA), error correction, control for DDC execution of commands, status monitoring, and diagnostic self-test routines. Drive dependent tasks performed by the DDC involve manipulation of the data stream necessary to read or write data on the disc. These operations include serialization/deserialization, modified frequency modulation (MFM) encoding/decoding, DMA handshaking, and error detection.

Associated with the DDC is a disc drive assembly which contains a sealed head-disc module and electronic control and read/write circuits. These circuits operate in conjunction with the circuitry in the DDC to interpret and generate control signals, position and maintain the read/write heads over the desired track, maintain precise disc rotational speed, and perform read and write operations.

The HDC is capable of interfacing with a second mass storage device, such as a cartridge tape drive, fitted with a suitable DDC. This facilitates, with a minimum of additional electronic circuitry, the connection of the cartridge tape drive as a back-up device. The back-up function is not implemented in the HP 7941 and HP 7945 Disc Drives.

The HDC communicates with the host computer over the Hewlett-Packard Interface Bus (HP-IB) and with the DDC's over the mass storage structure's Data/Control Interface Bus (DC-IB). The DC-IB contains an 8-bit read/write data bus, and a completely independent 8-bit control/status data bus with associated 6-bit control/status address bus. The DDC communicates with the disc drive assembly via the data and control lines of the ST-506 Interface. The ST-506 Interface is an electrical and mechanical standard for disc drives established by the Shugart Corporation and adapted as an industry-wide standard.

The disc drive consists of host dependent controller printed-circuit assembly (PCA) A5, device dependent controller PCA-A2, disc drive assembly A1, and power supply assembly A4. Disc drive assembly A1 and power supply assembly A4 are mounted side by side at the bottom of the cabinet and PCA's A2 and A5 are mounted horizontally above them. The four assemblies are connected together by cable assemblies.

Circuits on the host dependent controller PCA-A5 include an HP-IB interface integrated circuit (IC), a microprocessor, firmware in erasable programmable read-only memory (EPROM), random-access read/write memory (RAM), a custom-designed DMA gate array IC, and self test switches and display. Device dependent controller PCA-A2 includes a disc controller IC and a phase-locked loop (PLL) IC. Disc drive assembly A1 contains a sealed head-disc module with spindle motor, discs, read/write (R/W) heads, a servo head, read preamplifier/write driver IC's, a servo preamplifier IC, a rotary voice-coil head positioning mechanism (actuator), and air filtration components. Also located in disc drive assembly A1 are a microprocessor and programmed logic array (PLA), a read/write data channel, and circuits for actuator servo control and spindle speed control. Power supply assembly A4 is a self-contained switch-mode power supply which supplies dc voltages and a power-on reset signal to the disc drive.

A typical operation of the disc drive, locate and read, is performed as follows: The locate and read command from the host computer enters the HDC HP-IB interface IC, is stored in RAM, and interpreted by the HDC microprocessor. The HDC microprocessor executes code from the executive (EXEC) firmware in EPROM to carry out its control and management functions. The exec code in EPROM directs the DDC 0 (disc drive) code in EPROM to execute commands necessary for command completion. The DDC 0 EPROM firmware controls the disc drive assembly via the DC-IB bus and the DDC.

The DDC is given the seek argument, which causes the disc controller IC in the DDC to drive the actuator servo control in disc drive assembly A1 via its microprocessor and PLA with a stream of pulses which represents the seek offset argument. Once on track, the DDC verifies the locality from information on the data track. If the head is on the proper track, the disc rotates until the correct sector is read. The MFM-encoded serial data stream from the disc passes from the read/write head through the read preamplifier/write driver IC and the read/write data channel to the DDC PLL IC and disc controller IC. Here the MFM data is decoded and packed into bytes. These bytes are sent to the HDC RAM, previously assigned by the HDC microprocessor via the DMA gate array IC. As th data is being assembled, it is checked, one sector at a time, for errors. Errors are corrected in the HDC using information supplied by the disc controller IC. The HDC exec firmware coordinates the transfer of data from the RAM to the host computer via DMA gate array IC and the HP-IB interface IC.

The operation continues until the requested amount of data has been successfully read, assembled, checked for errors, buffered in RAM, and sent to the host computer. When the data transfer is complete, the DDC gives ending unit status to the exec code. The ending status is sent to the host computer.

A locate and write operation is similar to the locate and read operation previously described except for the direction in which the user data flows. The set up and head positioning operations are the same. However, the data is accepted into the RAM from the HP-IB interface IC prior to the seek and verify operation. This is done to allow the data to start moving from the RAM through the DDC disc controller IC serializer and formatter, and the disc drive read/write channel as quickly as possible once it is determined that the head is in the proper position.

Included in the HDC firmware are diagnostic self-test routines which exercise key functions of the disc drive and indicate faults on a 2-digit hexadecimal display which is visible through an opening in the rear panel of the disc drive. Also, a front panel FAULT/ON LINE indicator driven by DDC PCA-A2 shows the operating status of the drive. The disc drive has dedicated maintenance tracks where the results of some of the self tests are logged. The internal diagnostics permit off-line testing of the HDC, DDC, disc drive assembly, and power supply. This furnishes a quick and easy means of fault isolation to the unit, assembly, and subtest level. An additional troubleshooting aid is provided by a CS/80 External Exerciser which links the disc drive internal diagnostics and utility programs to service-trained personnel. The CS/80 External Exerciser can also be used to check the HP-IB channel and the interaction of the disc drive with the system host.

The disc drive circuitry is discussed in this section, first at a basic block diagram level and then at a more detailed functional block diagram level. A description of the disc recording format is also provided.

In order to facilitate text references to the three sheets of the functional block diagram (figure 3-4), each sheet is identified by a large numeral in the lower right-hand corner of the page. These numerals are printed in boxed characters in the text, for example: **1B** .

The mnemonics used in the functional block diagram and accompanying text to identify analog and digital signals are defined in table 3-1. In the "Source" column of table 3-1, the assembly where the signal originates is listed , followed by a boxed numeral identifying the sheet of the functional block diagram where the assembly is shown.

Most of the mnemonics listed in table 3-1 have "-L" or "-H" suffixes. These suffixes identify active low or active high logic signals, respectively. Signals without such suffixes are usually bus or analog signals.

In addition, section IV, Service Information, contains system cabling and signal distribution diagrams for the disc drive.

3-2. DISC FORMAT

The two plated metal discs in disc drive assembly A1 (HP 7941) provide three data surfaces, each with one read/write head. The fourth surface is used with a servo head for prerecorded servo data. The four discs in the HP 7945 provide seven data surfaces and one servo surface. See figure 1C.

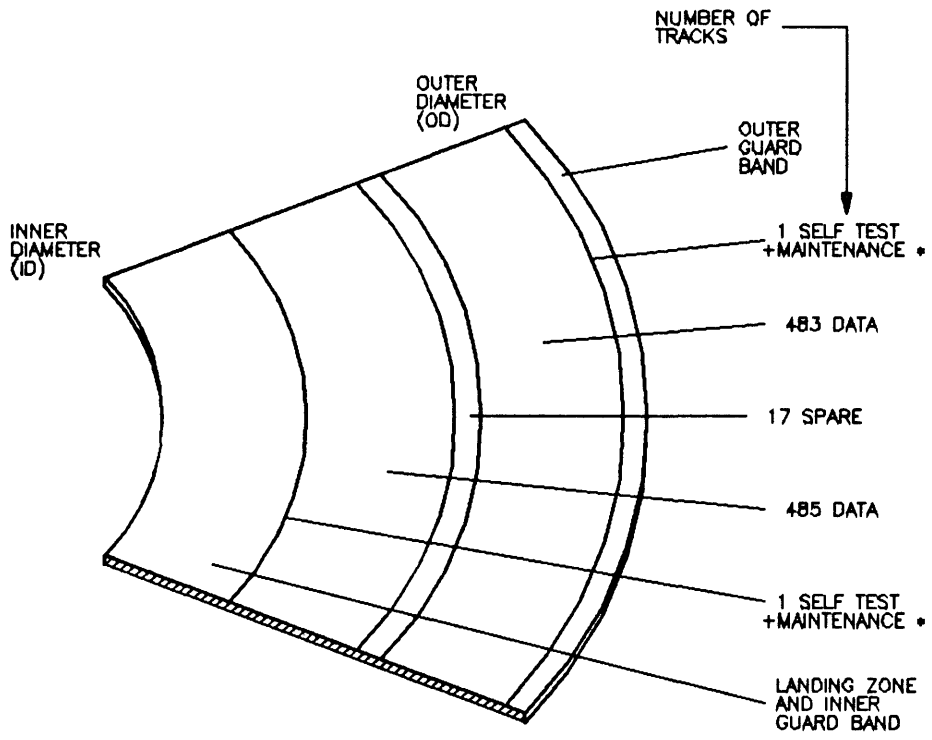
Each data surface is divided into 987 concentric circles called tracks. See figure 3-1. From the outside diameter of the disc there are: one self-test/maintenance track, 483 data tracks, 17 spare tracks, 485 data tracks, and one self-test/maintenance track.

The two self test/maintenance tracks are used for testing reading and writing. These tracks also contain service information, including run time logs, fault logs, and a spare table directory. See figure figure 3-1. The self test/maintenance tracks are located at the inner diameter (ID) and outer diameter (OD) of the disc to permit read/write testing at these locations. Also, duplicating the service information at two locations reduces the possibility of loss of data due to recording medium failure. The 968 data tracks are used for reading and writing data. This provides the user with 968 addressable cylinders. The 17 spare tracks are used for sparing out tracks containing hard errors.

Each data track is organized into smaller sequentially-numbered blocks of data called sectors. Figure 3-2 shows the track format, based on 32 data sectors, each having 256 bytes of data information. The beginning of each sector is identified by a prewritten identification (ID) field which contains the physical sector address plus cylinder and head information. This ID field is followed by the data field. The beginning of both the ID field and the data field is flagged by unique two-byte characters called address marks. The first byte in both address marks is a hexadecimal A1 pattern. This is followed by a FE pattern for the ID address mark and an F8 pattern for the data address mark.

A summary of the recording capacity provided by user available data tracks in the HP 7941 and HP 7945 is provided below.

	Data Bytes Per	Sectors Per	Tracks Per	Heads Per
Sector	256			
Track	8,129	32		
Head	7,929,856	30,976	968	
7941	23,789,568	92,928	2,904	3
7945	55,508,992	216,832	6,776	7



*SELF TEST AND MAINTENANCE TRACK CONTENTS:

SECTOR ADDRESS	OUTER DIAMETER (OD)	INNER DIAMETER (ID)
0	PRODUCT NO.	SERIAL NO.
1–5	RUN TIME LOG	RUN TIME LOG
6–10	ERROR RATE TEST (ERT) LOG	ERROR RATE TEST (ERT) LOG
11–15	FAULT LOG	FAULT LOG
16–18	SPARE TABLE	SPARE TABLE
19–20	SELF TEST LOCATION	SELF TEST LOCATION
21–22	SELF TEST LOCATION	SELF TEST LOCATION
23–31	NOT USED	NOT USED

FILE=FSJEF12A

Figure 3-1. Disc Recording Format

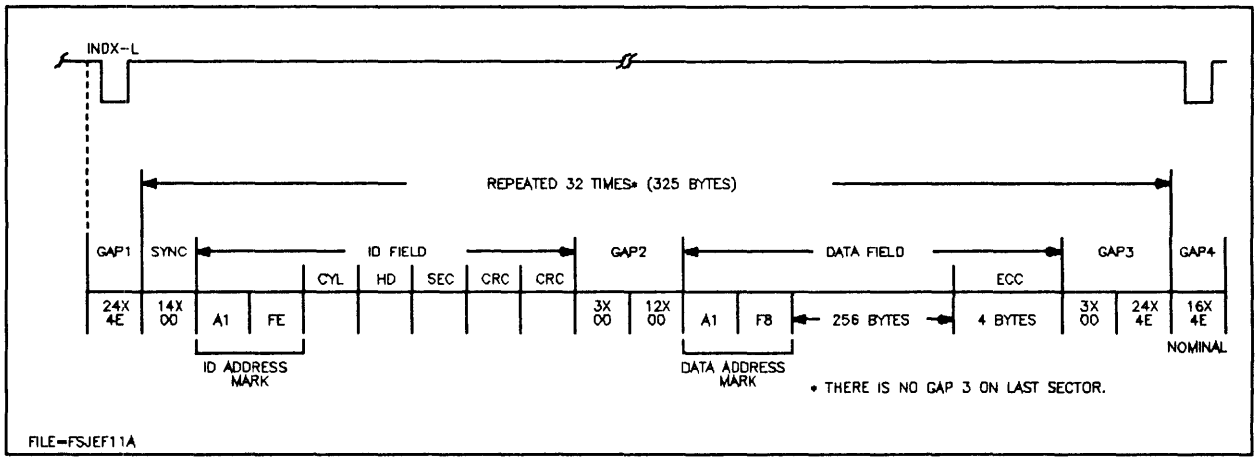


Figure 3-2. Track Recording Format

3-3. HDC PCA-A5

Host dependent controller PCA-A5 provides an interface between the host computer and the device dependent controller (DDC) of the disc drive. (The HDC is also capable of interfacing with the DDC of a second mass storage device. This feature is not used in the HP 7941 and 7945.) The common functions required for the two mass storage devices are consolidated in the HDC leaving the device dependent tasks (servo control, read, write, data separation, data generation etc.) to the DDC's. Host dependent controller interface with the host is via the Hewlett-Packard Interface Bus (HP-IB) and with the DDC's via the HDC's Data/Control Interface Bus (DC-IB).

Host dependent controller functions include:

- A host interface via the HP-IB.
- Direct memory access (DMA) capability.
- A random access memory (RAM) buffer for data examination for integrity, error correction, and speed matching between devices.
- Firmware for a microprocessor to execute DDC commands and monitor status.
- Self-test diagnostic capabilities.

Circuits in host dependent controller PCA-A5 (see figure 3-3) include an HP-IB interface IC, a microprocessor, firmware in EPROM, RAM, a custom-designed DMA gate array IC, and self-test switches and display.

The firmware in the HDC consists of three segments. One segment is the executive operating system (EXEC EPROM) which controls resource allocation (including the DMA gate array IC and RAM), and the passing of messages and information between the DDC firmware and the host interface firmware. The remaining two segments comprise the control firmware for the two mass storage devices (DDC 0 and DDC 1). The microprocessor is shared between the two sets of DDC firmware and the executive firmware by timesharing, each receiving the microprocessor for approximately 0.5 millisecond. Each set of firmware takes care of its own task, performing whatever function the host or device has requested. Self-test firmware is included in each of the three segments. The DDC's communicate with the HDC over the DC-IB. This bus contains an 8-bit control/status data bus with appropriate read/write strobes and associated 6-bit control/status address bus, and a completely independent 8-bit read/write data bus with associated strobes.

The following paragraphs provide a more detailed description of the host dependent controller circuitry, as shown on the disc drive functional block diagram, sheet 1A . Refer to table 3-1 for a description of the mnemonics used in the text and on sheet 1A

3-4. HDC INTERNAL BUS ARCHITECTURE

The internal bus architecture of the HDC consists of the following buses:

- HP-IB Data Bus

- RAM Data Bus
- Microprocessor Address Bus
- Microprocessor Data Bus
- DMA Gate Array Data Bus
- Read/Write Data Bus

A brief description of the function of each internal bus is provided in the following paragraphs.

3-5. HP-IB DATA BUS. The HP-IB Data Bus is accessed by the microprocessor and by the DMA gate array IC input and output processes. The microprocessor must read and write to the various registers in the HP-IB interface IC in order to prepare for data transfers to and from the host computer. Buffers separate the HP-IB Data Bus from the RAM Data Bus and permit speed matching between the HP-IB data rate and the DMA gate array IC data transfer rate.

3-6. RAM DATA BUS. The RAM Data Bus is used for all data transfers between the RAM and the microprocessor, the RAM and the DDC's, and the RAM and the HP-IB. The use of the RAM is time multiplexed , so that in one half of the microprocessor clock cycle, the microprocessor has access to the RAM, and in the other half, the DMA gate array IC has access to the RAM.

3-7. MICROPROCESSOR ADDRESS BUS. The Microprocessor Address Bus points to the next instruction or data source. The circuits addressed by the Microprocessor Address Bus include the HP-IB interface IC, RAM (via the address multiplexer), DMA gate array IC, EXEC EPROM, DDC 0 EPROM, and DDC 1 EPROM. The DDC EPROM's are overlaid on the same address space. A EPROM switch selects the DDC 0 EPROM or the DDC 1 EPROM when the time interval for DDC 0 or DDC 1 occurs. The microprocessor can write directly to one or two DDC's via a buffer and the DC-IB Control/Status Address Bus to operate the mass storage units.

3-8. MICROPROCESSOR DATA BUS. The Microprocessor Data Bus interconnects the microprocessor, the EXEC EPROM, the DDC 0 EPROM, and the DDC 1 EPROM. The microprocessor RAM exists on a separate bus so that the RAM can be shared by the microprocessor and the DMA gate array IC. The bidirectional data on the Microprocessor Data Bus includes preprogrammed control sequences (algorithms) in EPROM and control/status information from the DDC's. The Microprocessor Data Bus is connected to the DDC's via a bidirectional buffer and the DC-IB Control/Status Data Bus.

3-9. DMA GATE ARRAY DATA BUS. The DMA Gate Array Data Bus is used when the microprocessor must read or write to registers in the DMA gate array IC, including the DMA registers and the free-running timer used to sequence between executive, DDC 0, and DDC 1 operations.

3-10. READ/WRITE DATA BUS. The Read/Write Data Bus is used to pass data to and from the chosen DDC. External to the HDC, the bus becomes the Read/Write Data Bus portion of the Data/Control Interface Bus (DC-IB) linking the HDC to the DDC's.

3-11. DATA/CONTROL INTERFACE BUS

The Data/Control Interface Bus (DC-IB) is the communication link between the HDC and the DDC's. The DC-IB consists of two independent data buses -- a Control/Status Data Bus and a Read/Write Data Bus.

The Control/Status Data Bus is used to send commands to a DDC such that it can initiate the transfer of information to or from the recording medium, or it can be used to interrogate the status of the DDC and its drive mechanism. A Control/Status Address Bus associated with the Control/Status Data Bus provides an addressing capability.

The Read/Write Data Bus is the path taken by all the data which flows between the host computer and the DDC. Details of these DC-IB signals, and their associated select and strobe lines are given in the following paragraphs.

3-12. CONTROL/STATUS DATA BUS. Control/Status Data Bus, Bits CSB0-H through CSB7-H comprise a bidirectional 8-bit data bus which is used to pass control and status information between the HDC and a given DDC.

3-13. CONTROL/STATUS READ STROBE. Control/Status Read Strobe signal CSRS-L is used to pass bytes to the HDC across the Control/Status Data Bus. These bytes will be of a DDC-status nature since the actual recording medium information will be passed over the Read/Write Data Bus.

3-14. CONTROL/STATUS WRITE STROBE. Control/Status Write Strobe signal CSWS-L is used to pass bytes from the HDC to the DDC across the Control/Status Data Bus.

3-15. CONTROL/STATUS ADDRESS BUS. Control/Status Address Bus, Bits CSA0-H through CSA5-H are the address lines associated with the Control/Status Data Bus. The address lines are used to access specific registers in the DDC's attached to the DC-IB.

3-16. SELECT. Select signal SEL-L chooses which DDC will respond to a given Control/Status Data Bus operation. A low-level SEL-L selects DDC 0 (disc drive).

3-17. READ/WRITE DATA BUS. Read/Write Data Bus, Bits DATA0-H through DATA7-H comprise an 8-bit bus used to pass high-speed data between the HDC and the chosen DDC. The data on the bus is the digital information going to and coming from the recording medium.

3-18. DATA REQUEST IN/DATA REQUEST OUT. Data Request In signal DRIN-L and Data Request Out signal DROUT-L are 3-state DMA request lines used to transfer bytes over Read/Write Data Bus DATA0-H through DATA7-H. The "out" direction is defined as being from the HDC to the DDC. A DDC is programmed via the Control/Status Data Bus to drive a given request line.

3-19. DATA STROBE IN/DATA STROBE OUT. Data Strobe In signal DSIN-L and Data Strobe Out signal DSOUT-L are HDC-generated DMA strobe lines which accompany the transferring of data between the HDC and the DDC.

3-20. HP-IB INTERFACE IC

The HP-IB interface integrated circuit is a talker/listener device. This IC provides the interface between the host data channel (HP-IB) and the mass storage device. The IC is accessed by the microprocessor and by the DMA gate array IC input and output processes. The microprocessor must read and write to the various registers in the HP-IB interface IC in order to prepare for data transfers to and from the host computer. Buffers separate the HP-IB data bus from the RAM data bus.

The HP-IB interface IC implements all of the talker/listener functions of the HP-IB including data transfers, handshake protocol, talker/listener addressing, service request, and serial and parallel polling. HP-IB signals connected to the IC include HP-IB Data I/O Bus DIO1-L through DIO8-L, End or Identify EOI-L, Data Valid DAV-L, Not Ready for Data NRFD-L, Not Data Accepted NDAC-L, Interface Clear IFC-L, Attention ATL-L, Service Request SRQ-L, and Remote Enable REN-L. The functions of these signals are described in Table 3-1.

3-21. MICROPROCESSOR

The microprocessor provides overall control of all device functions. The host dependent controller employs an internal 8-bit microprocessor. Firmware associated with the microprocessor includes the EXEC EPROM, the DDC 0 EPROM, and the DDC 1 EPROM. The EXEC EPROM and the DDC 0 EPROM provide approximately 44 kilobytes of code.

3-22. HP-IB ADDRESS SWITCH

The HP-IB ADDRESS switch is a 4-segment switch which is accessible to the operator through an opening on the rear panel of the disc drive. Three of the segments allow an HP-IB device address in the range of 0 through 7 to be set. The fourth segment on the switch is not used.

3-23. CHANNEL STATUS

The channel status block provides the microprocessor with information regarding the current status of the DMA gate array IC (DMA full, DMA not full) and details of the units connected to the HDC via the DC-IB.

3-24. SELF-TEST SWITCHES

Two momentary contact pushbutton switches, accessible through openings in the rear panel of the disc drive, allow the operator to initiate operation of the internal self-test diagnostic routines. One

switch, labeled SELF TEST, initiates the self-test routines. The other switch, labeled DISPLAY RESULTS, causes the self-test results to be displayed on the self-test display. The microprocessor can read the operation of the switches and will initiate the appropriate self-test operations.

3-25. SELF-TEST DISPLAY

The Self-Test display consists of two 7-segment LED's which are visible through openings in the rear panel of the disc drive. The display is controlled by the microprocessor and provides a 2-digit hexadecimal readout of self-test results, including the defective unit, field replaceable assembly (FRA), and subtest failure number. Information on how to interpret the self-test readout is contained in section IV, Service Information.

3-26. DMA GATE ARRAY IC

The DMA (direct memory access) gate array IC is a custom-designed integrated circuit which performs the DMA function for the host dependent controller. DMA is defined as the ability to perform complete memory cycles without the intervention of the HDC microprocessor. The DMA gate array IC controls data transfers between the host and RAM. It also transfers self-test status information from the microprocessor to the self-test display. The DMA gate array is set up for either an input to or an output from the RAM. Once activated, the DMA gate array IC performs reads or writes to the RAM completely transparent to the microprocessor.

3-27. RAM

The random access memory (RAM) is a temporary storage location for all data transfers. The use of RAM is time multiplexed, so that for one half of a microprocessor clock cycle, the microprocessor has access to RAM; for the other half, the DMA gate array IC has access to RAM.

3-28. EXEC EPROM

The executive (EXEC) EPROM contains the firmware which controls operation of the HDC microprocessor and the interface with the host computer. This includes decoding and validating host commands, and setting up the data transfer paths. The EXEC EPROM employs a 16k by 8 EPROM. All 16k is used.

3-29. DDC 0 EPROM

The device dependent controller (DDC) 0 EPROM contains firmware which provides permanent storage for the preprogrammed sequences which govern operation of the DDC for unit 0 (disc drive). The EPROM is addressed by the Microprocessor Address Bus via the EPROM switch and information is sent out over the Microprocessor Data Bus. The DDC 0 EPROM module is overlaid on the same address field as the DDC 1 EPROM. A EPROM switch selects the DDC 0 EPROM or DDC 1 EPROM when the time interval for the microprocessor to have access to DDC 0 or DDC 1 occurs. The DDC 0 EPROM employs two EPROM's. A total 28k of the available 32k is used.

3-30. DDC 1 EPROM

The DDC 1 EPROM contains firmware for controlling a second mass storage device. This function is not implemented in the HP 7941 and HP 7945 Disc Drives.

3-31. ADDRESS MULTIPLEXER

The address multiplexer (MUX) allows the RAM addresses to be multiplexed between the microprocessor and the DMA gate array IC.

3-32. CLOCKS AND CONTROL LOGIC

The clocks and control logic block contains all of the circuitry controlling the timing and operation of the host dependent controller.

3-33. ROM SWITCH

The ROM switch allows access to the DDC 0 or DDC 1 firmware so that either code can be executed. This permits the firmware to be larger than the linear address space of the microprocessor.

3-34. BUFFERS

The buffers consist of a number of unidirectional and bidirectional buffers which provide the required communication and isolation between the various buses of the HDC. On sheet 1A, unidirectional buffers are identified by a single arrow and the bidirectional buffers by dual arrows.

3-35. TYPICAL HDC TRANSACTION

The following is a description of a typical HDC transaction -- the flow of data between the host computer and the disc drive. To start the process, the host computer sends a command to the disc drive asking for the transfer of a sector of information to the host. The command is received by the HDC executive firmware and the command is validated. The command is then passed to the disc drive DDC firmware (DDC 0) in the form of a message. The message is received and the disc drive firmware issues seek and read commands to its DDC servo and read/write circuitry. Also, the disc drive firmware requests from the executive firmware an input channel to the DMA gate array IC and a buffer in RAM. When allowed to do so, the disc drive firmware programs the DMA gate array IC for an input transfer. In conjunction with this action, a request is made to the executive firmware for the use of the DMA gate array IC output channel, which will transfer data from RAM to the HP-IB interface IC.

When a RAM buffer is full of data from the disc, the buffer is given the process that will output the buffer to the HP-IB interface, with the executive firmware starting the buffer transfer. Multiple buffers may be transferred. The DMA gate array IC transfers the data from the RAM to the host computer and terminates the operation when the buffer is empty. The host computer interrogates the HDC as to the status of the transfer, which the HDC returns to the host. This completes the host computer's request for disc information.

3-36. DDC PCA-A2

Device dependent controller (DDC) PCA-A2 performs the following functions in the peripheral mass storage control structure used in the disc drive:

- Accepts high-level disc drive control commands issued by the host dependent controller (HDC) over the DC-IB bus, and provides high-level status commands to the HDC.
- Executes these high-level commands by transferring them into ST-506 Interface control sequences.
- Performs all of the manipulations of the data stream necessary to read or write data on the disc. Functions required for this manipulation include serialization/deserialization, MFM encoding/decoding, error detection, DMA data transfer handshaking, and write precompensation.

Circuits in the DDC include a disc controller IC and and a phase-locked loop IC. Additional support circuitry includes controller and register decode logic, four registers for disc controller IC backup and control, a clock generator, and write precompensation.

The following paragraphs provide a more detailed description of the device dependent controller circuitry, as shown on the disc drive functional block diagram, sheet 1B . Refer to table 3-1 for a description of the mnemonics used in the text and on figure 1B .

3-37. HDC/DDC COMMUNICATION

Communication between the HDC and the DDC takes place via the Data/Control Interface Bus (DC-IB). The DC-IB provides three primary buses for passing control/status information and data to be stored or retrieved. These are:

- Control/Status Data Bus
- Control/Status Address Bus
- Read/Write Data Bus

A brief description of the function of each bus, as related to the operation of the DDC, is provided in the following paragraphs.

3-38. CONTROL/STATUS DATA AND ADDRESS BUSES. All disc drive high-level control commands and status information are passed to/from the DDC via Control/Status Data Bus, Bits CSB0-H through CSB7-H and Control/Status Address Bus, Bits CSA0-H through CSA5-H. Control and status information ultimately resides in specific registers in the DDC. The Control/Status Address Bus is a unidirectional bus since it passes only address information. The actual values sent or received from a register are sent over the Control/Status Data Bus. This bus is a bidirectional bus since data can be sent or received over it.

To send control/status information to the DDC, the target register is addressed with the

Control/Status Address Bus, the data to be written to the register is placed on the Control/Status Data Bus, Select signal SEL-L is set low, and Control/Status Write Strobe CSWS-L is pulsed.

To retrieve information, the target register is addressed with the Control/Status Address Bus, Select signal SEL-L is set low, and Control/Status Read Strobe CSRS-L is pulsed. As CSRS-L is pulsed, the register value is placed on the Control/Status Data Bus.

3-39. READ/WRITE DATA BUS. Disc storage data to be stored or retrieved is passed over Read/Write Data Bus DATA0-H through DATA7-H. When a command requires data to be transferred, the data is passed on the Read/Write Data Bus, one byte at a time, and clocked in or out using the appropriate DMA handshake lines DRIN-L, DSIN-L, DROUT-L, or DSOUT-L.

When writing data to the disc, the HDC places the first byte of the transfer on the Read/Write Data Bus. However, the actual transfer of data does not begin until the DDC is ready to accept data (that is, the disc has arrived at the target sector). When ready to accept data, the DDC activates Data Request Out line DROUT-L. When the HDC senses DROUT-L, it pulses Data Strobe Out line DSOUT-L, clocking the byte out from the HDC onto the Read/Write Data Bus. This DROUT-L/DSOUT-L handshake continues until the transfer length determined by the sector count register in the disc controller IC has been satisfied.

When reading data from the disc, the Data Request In DRIN-L and Data Strobe In DSIN-L lines are used to handshake data into the HDC from the DDC.

In both the write and read operations described above, the Data Request lines signal the readiness of the DDC to transfer a byte. Data Strobe lines are activated by the HDC to clock data in or out.

3-40. RECEIVER/DRIVER. Two different types of receivers and drivers are employed in the DDC. The receiver and driver used to provide a bidirectional data transmission path for Read/Write Data Bus DATA0-H through DATA7-H between the DDC and the HDC consist of two identical octal D-type flip-flop devices with 3-state outputs. The receiver used for unidirectional input of Control/Status Address Bus CSA0-H through SCA5-H and Select line SEL-L consists of an octal buffer/line driver with 3-state outputs.

3-41. TRANSCEIVERS. Bidirectional transmission of Control/Data Bus CSB0-H through CSB7-H between the DDC and the HDC takes place via an octal transmitter/receiver designed for asynchronous 2-way communication. A line from the controller IC and register decoder logic block to the transceiver determines the direction of signal transmission. A similar transceiver is used to manage control status information to the disc controller IC and disc data which passes through the disc controller IC.

3-42. DDC/DISC DRIVE A1 COMMUNICATION

Communication between the DDC and disc drive assembly A1 takes place via the ST-506 Interface. This function is provided primarily by the disc controller IC and some additional support circuits.

The ST-506 Interface signals are divided into two groups -- control and data. Signals in the control group include Head Select Bits HS0-L through HS8-L, Seek Complete SKCMP-L, Track 0 TRK0-L, Write Fault WFLT-L, Index INDX-L, Ready RDY-L, Step STEP-L, Direction DIR-L, Write Gate WGATE-L, and Drive Select Bit DS0-L.

Signals in the data group are differential MFM Write Data lines WMFM+, WMFM- and differential MFM Read Data lines RMFM+, RMFM-.

The functions of the ST-506 Interface control and data signals are described in table 3-1, List of Mnemonics.

3-43. CONTROLLER IC AND REGISTER DECODE LOGIC

The controller IC and register decode logic controls selection of the disc controller IC and a number of registers external to the disc controller which provide additional control, management, and status functions. Inputs to the decode logic are Control/Status Address Bus, Bits CSA0-H through CSA5-H, Control/Status Read Strobe CSRS-L, Control/ Status Write Strobe CSWS-L and Select line SEL-L. The registers controlled by the decode logic include one PROM, four general purpose

registers, and two test registers. Details of these components are provided in the following paragraphs.

3-44. HDA DESCRIPTION PROM. The HDA description PROM is a 512-byte programmable read only memory containing all of the information necessary to describe the head-disc module contained in disc drive assembly A1 to the HDC. Each head-disc module described in the PROM has two 32-byte description fields containing device specific information. One field is selected for normal operation and the other field is reserved for factory use. The desired field is selected with 4-segment switch U484 on the DDC. The switch settings for normal operation of the HP 7941 and HP 7945 are noted in section V of this manual.

3-45. SELF-TEST REGISTER. A general-purpose read-only register which contains self-test information.

3-46. GPC REGISTER. A general-purpose write-only register which performs hardware control functions. The register provides drive for the front panel FAULT/ON LINE indicator via outputs RED-L and GREEN-L.

3-47. DDC ERRORS REGISTER. A general-purpose read register which contains DDC error/fault descriptions and DMA data transfer information.

3-48. PUPO REGISTER. A general-purpose read/write register which acts as an overflow for DMA data transfer sector counting. The mnemonic PUPO represents Protect Under/Protect Over.

3-49. DISC CONTROLLER IC

The disc controller IC is a single-chip IC which provides most of the control signals to manage the ST-506 Interface. To perform disc storage functions, command information is written into registers in the disc controller via the Control/Status Interface Bus (DC-IB). At the end of the command, the disc controller carries out the command by manipulating the ST-506 Interface and the DMA control lines, as needed. Operation of the disc drive begins when the HDC initiates a command by loading the internal registers in the disc controller. Information such as cylinder, sector, and head number is written to these registers with the selected address lines. The disc controller is run by an internal programmed logic array (PLA) which controls the flow of data through the chip, recognizing the commands and formatting the data.

During a write operation, parallel data is read from the Read/Write Data Bus and written to a specific sector. However, before the write operation can begin, the cylinder and sector must be located. The disc controller consults its internal cylinder position information and compares it with the requested cylinder number. If necessary, a seek is performed to position the head over the desired track. After the disc controller finds an ID field which matches the cylinder, head, and sector, the disc controller reads parallel data in from the Read/Write Data Bus, serializes it, converts it into an MFM format, and sends it to the ST-506 Interface to be written on the disc. If the original command specified multiple sectors, the next logical sector must be searched for and the process is repeated. After the last sector is written, the disc controller returns the bus back to the HDC.

The read operation is similar to the write operation, except that decoded data is sent out on the Read/Write Data Bus and written into RAM in the HDC. MFM-encoded read data is entered into the disc controller over the differential RMFM+, RMFM-lines together with a synchronous clock generated by the external phase-locked loop IC.

The controller includes error correction code (ECC) logic which provides data error detection capabilities and in addition, can support data error corrections. This function provides the capability to detect errors of up to five consecutive bits in length anywhere within a full sector.

The disc controller computes four ECC bytes for each sector and appends these bytes to the end of each data field during sector write operations. During sector reads, the disc controller computes four error syndrome bytes. These error syndrome bytes are then used to compute correction information if an error occurs.

Error detection is signaled when an error control line in the logic goes active. This error status line runs to the DDC errors register. Host firmware can recognize a data error by examining bit 5 of the DDC errors register.

Error correction is performed by using information supplied by the disc controller. When a data error arises, the disc controller makes information available to the HDC that tells a) the location of the error within the sector (error offset), and b) the error pattern required for correction. HDC firmware uses this information to correct data errors within the target sector.

The ECC function can be operated in a standard "generation" mode or in a "long" mode, as selected by the GPC register. In the "generation" mode, the ECC bytes are generated by the disc controller and applied to the data field during sector writes. Also, syndrome bytes are stored in the disc controller for subsequent reading upon detection of a data error. In the "long" mode, ECC or syndrome bytes are not generated by the disc controller. Instead, the user can issue four bytes to be appended on a sector during writes. In the "long" mode, the four bytes following the data field are passed directly back to the user and are not used for syndrome generation. The "long" mode is employed for diagnostic checkout of the ECC hardware and firmware; it is not used during normal operation of the disc drive.

3-50. PHASE-LOCKED LOOP IC

The data separation function of the disc controller IC is implemented with a phase-locked loop (PLL) IC. The PLL separates the clock and data pulses contained in the raw MFM-encoded read data signal. This signal, received from the read chain in disc drive assembly A1, is labeled RMFM+, RMFM-. The PLL IC passes synchronized data and a read clock to the disc controller IC where the actual data separation and byte packing takes place.

3-51. LATCH

The latch is an octal D-type flip-flop which latches in head and disc drive information which is supplied to the ST-506 Interface. This latch is necessary since the disc controller IC does not supply these signals. Outputs are Drive Select line DS0-L and Head Select signals HS0-L through HS8-L.

3-52. DMA HANDSHAKE CONTROL

The DMA control logic includes the circuits needed to: interface with the DMA operation; supply Data Request signals DRIN-L, DROUT-L; and accept Data Strobe signals DSIN-L, DSOUT-L. Disc data is transferred to/from the disc one byte at a time via the drivers and receivers on Read/Write Data Bus DATA0-H through DATA7-H.

3-53. CLOCK GENERATOR

The clock generator supplies a 5-MHz clock signal to the disc controller IC to synchronize write operations. The generator also provides a 10-MHz clock input to the phase-locked loop IC in the data separator circuit.

3-54. WRITE PRECOMPENSATION

Because of the multiple frequency content of the MFM-encoded data, the transitions written on the disc are not equally spaced. During readback, pulse crowding causes the transitions to move from their expected position. To compensate for timing shift and prevent this pulse crowding, write data timing is adjusted prior to the write operation.

Write precompensation is provided in the DDC by data lines and control logic external to the disc controller IC. The disc controller provides lines to control the external precompensation circuitry. These lines are used to select the proper delay depending upon the MFM sequence being written. Since pulse crowding does not occur in disc drive assembly A1, the write precompensation circuit is bypassed. (Precompensation circuitry is included in the DDC to ensure compatibility with future products.)

3-55. DISC DRIVE A1

Disc drive assembly A1 consists of a sealed head-disc module containing a rotary voice-coil head positioning mechanism (actuator), recording medium, read/write heads, a servo head, a spindle motor, and air filtration components. Also included in assembly A1, external to the head-disc module, are two PCA's which contain read/write, servo, and interface control electronics.

The components in disc drive assembly A1 perform the following functions:

- Perform a power-on self-test.
- Interpret and generate control signals.
- Position and maintain the read/write heads over the desired track.
- Maintain precise disc rotation speed.
- Read and write MFM-encoded data.
- Report write faults.
- Provide a contamination free environment for the actuator, recording medium, and heads.

The electronics are packaged on two PCA's. The outermost PCA on the assembly, to which the ST-506 control and data signals are connected, includes: read/write circuits, interface drivers and receivers, microprocessor control logic, write fault detection, drive selection, and an index circuit.

The second PCA, mounted under the outermost PCA, accepts +5V from power supply assembly A4 and performs the following functions: spindle speed control, head actuator positioning, track 0 detection, power reset, and clock generation.

Interpretation and generation of control signals are performed by a microprocessor and a programmable logic array (PLA). Positioning of the heads is achieved by driving the actuator with a dedicated track-following servo system. Speed control of the spindle motor is performed by a phase-controlled driver circuit using a 360-Hz reference signal. MFM-encoded data is written to and read from the discs by means of a read/write data channel. Write errors are reported by read preamplifier/write driver IC's in the read/write data channel. Contamination protection for the heads, actuator, and recording medium is achieved by enclosing these components in a sealed head-disc module having a built-in air filter.

The following paragraphs provide a more detailed description of the disc drive assembly A1 components and electronic circuits, as shown in the disc drive functional block diagram, sheet 1C. Refer to table 3-1 for a description of the mnemonics used in the text and sheet 1C.

3-56. DISC DRIVE A1/DDC CONTROL COMMUNICATION

The ST-506 Interface control signals input to disc drive assembly A1 via input buffers are Step STEP-L, Drive Select DS0-L, Head Select HS0-L through HS8-L, Direction DIR-L, and Write Gate WGATE-L. These signals are applied to either the microprocessor or the PLA, as shown in sheet 1C

The ST-506 Interface control signals output from disc drive assembly A1 via output drivers are Seek Complete SKCMP-L, Track 0 TRK0-L, Write Fault WFLT-L, and Ready RDY-L. The majority of these signals are output by the microprocessor or the PLA. See sheet 1C.

Head Select lines HS0-L through HS8-L are applied via input buffers directly to head select and control logic which outputs Chip Enable signal CE, Write Select WS, and Head /Select lines HS1-H, HS2-H, to the read preamplifier/write driver IC's in the sealed head-disc module.

3-57. INPUT BUFFERS

The ST-506 Interface control signals from the DDC are input to the microprocessor and the PLA via input buffers.

3-58. OUTPUT DRIVERS

The ST-506 control signals from disc drive assembly A1 are output via open-collector drivers. Each driver is capable of sinking 48 milliamperes at its low level (true state) with a maximum of 0.4 volts measured at the driver. When the driver is in its high level (false state), the driver transistor is off. The output control signals are gated by a Drive Select line developed from the Drive Select input DS0-L.

3-59. DISC DRIVE A1/DDC DATA COMMUNICATION

Data signals passed between disc drive assembly A1 and the DDC are passed over the ST-506 Interface data lines. MFM Read Data signals RMFM+, RMFM- from the read/write data channel in A1 are output to the DDC via a differential line driver. MFM Write Data signals WMFM+, WMFM- from the DDC are input to the A1 read/write data channel via a line receiver.

3-60. MICROPROCESSOR AND PLA

Disc drive assembly A1 employs a microprocessor and a programmed logic array (PLA) to control its internal operations. These devices receive commands from the device dependent controller over the control lines of the ST-506 Interface bus. These operations include servo control, spindle speed control, read/write, and error/fault reporting.

The microprocessor consists of a single chip microcomputer IC which incorporates an 8-bit central processing unit (CPU), 4 kilobytes of program memory (ROM), 256 bytes of data memory (RAM), input/output lines, and a serial port. The microcomputer is clocked by an external 9.126-MHz clock generator. (This generator also provides 1152-kHz and 576-kHz signals for the actuator servo control demodulator and a 360-Hz signal for the spindle motor speed control circuit.)

The programmed logic array is a custom-designed IC which augments the operation of the microprocessor. Functions handled by the PLA include status logic, write fault monitor, read/write selection, and step control.

3-61. MICROPROCESSOR/PLA CONTROL SIGNALS

Signals generated by the microprocessor for control purposes within disc drive assembly A1 include: Seek, Odd In, Pick, Counter Reset, Normal Regulation, Stop Motor, Inner Track, Servo Enable, Even In, Velocity Command, Speed, and Seek Complete. PLA-generated signals include Write Gate, Seek Complete, Write Fault, and Ready.

Signals input to the microprocessor from circuitry internal to disc drive assembly A1 include: Power On Reset, Index, At Speed, Count Not Ready, Fault, Track 0, Off Track, On Peak, Direction In, Write Gate, and 9.216-MHz clock. Internal inputs to the PLA include Power On Reset, Fault, Write Gate, Drive Select, Stop, Seek Complete, and At Speed.

3-62. CLOCK GENERATOR

The clock generator consists of a crystal oscillator and a number of count-down registers. The clock generator has five outputs -- 9.216 MHz for the microprocessor, 1152 kHz and 576 kHz for the demodulator in the actuator servo control circuit, 92.1 kHz for the spindle speed checker circuit, and 360 Hz for the spindle speed control circuit.

3-63. HEAD-DISC MODULE

Details of the components contained in the sealed head-disc module are provided in the following paragraphs. See sheet 1C .

3-64. ACTUATOR. The read/write heads and servo head are mounted on a rotary arm supported by precision ball bearings. A bobbin-type voice coil, attached to the rotary arm, and mounted between two permanent magnets comprise a rotary voice-coil head positioning mechanism (actuator). This mechanism provides the driving force required to move the rotary arm for head positioning. The magnetic field in the gap between the magnets allows the acceleration of the rotary arm to be controlled by the voice-coil current. Drive current for the voice coil is supplied by the actuator servo control circuit. Crash stops are provided to protect the heads should a malfunction cause the actuator servo control circuit to lose control. When the disc drive is powered down, the rotary arm is driven to a nondata head landing zone at the inner diameter of the discs. Simultaneously, the arm is automatically locked over the landing zone to prevent possible head/medium damage if the disc drive is inadvertently subjected to excessive shock during relocation or shipment. Drive current for the actuator lock solenoid is supplied by an actuator lock driver circuit.

3-65. RECORDING MEDIUM. The recording medium is a plated metal magnetic coating on either side of a 130-millimetre (5.12-inch) diameter aluminum substrate. In the HP 7941, there are two such discs in the sealed head-disc module, with three surfaces used for data and one surface used for prerecorded servo information. The servo information is recorded on the lower surface of the bottom disc in the stack. In the HP 7945, there are four discs, with seven surfaces for data and one surface for servo information. Again, the servo information is recorded on the lower surface of the bottom disc in the stack.

3-66. READ/WRITE HEADS. The disc drive employs Winchester technology read/write heads, one for each data surface. The heads are designed to fly above the discs supported by a thin cushion of air which acts as an air bearing to the heads.

The flying height is approximately 16 microinches at the inner diameter of the disc. When the disc drive is powered down, the actuator moves the heads to the landing zone at the inner diameter of the discs where the heads come to rest on the surface.

Each head consists of a gapped ferrite core mounted in a ceramic slider. There are two windings wound around the ferrite core and the windings are connected at a common point and phased such that the common point acts as a center tap. These windings are used for both reading and writing by detecting or producing a magnetic field at the gap in the ferrite core.

In a write operation, data is written by passing a current through the windings of the selected head. This current generates a flux field across the gap and aligns the magnetic particles contained in the coating on the surface of the disc. The writing process orients the poles of each magnetized particle to store the direction of the flux field as the particles pass beneath the head. The direction of the flux field is a function of the write current direction. Erasing is accomplished by writing over any data which may have been previously recorded on the disc.

In a read operation, as the data surface passes beneath a head, the magnetically stored flux fields intersect the gap in the ferrite core. Gap motion through the flux field causes a voltage to be induced into the windings wound around the core. This induced voltage is analyzed by the read circuitry to define the data recorded on the surface of the disc. Each flux reversal, caused by a write current polarity change, generates a readback voltage pulse.

There are read preamplifier/write driver IC's mounted on the rotary arm of the actuator, adjacent to the heads. Each IC provides write current, head selection, and read signal amplification for four read/write heads. The IC's are connected to the read/write data channel electronics external to the sealed head-disc module via a flexible printed-circuit cable.

3-67. READ PREAMPLIFIER/WRITE DRIVER IC. The read preamplifier/write driver IC is standard integrated circuit designed for disc drive read/write head control. The IC can select 1 of 4 heads, read from or write to the selected head, and supply a write fault signal. One IC is used in the HP 7941. There are two IC's in the HP 7945. Control signals for the IC's are supplied by the head select and control logic block.

The IC is enabled by Chip Enable signal CE-L. Binary Head Select signals HS1-H, HS2-H are decoded by the IC to select the desired head. Reading and writing is controlled by Write Select signal WS. When WS is high, the write mode is selected, and when WS is low, the read mode is selected.

When the IC is in write mode, differential current applied across the DX, DY lines is used to switch the current drawn from the write current source to the head of the selected channel. Head voltage swings, generated by the switching of write current through the inductive head, are monitored by a head transition detect circuit in the IC. Absence of proper head voltage swings indicates an open or short in either half of the head winding, or an absence of write current. The absence of voltage swings will cause a current to flow into the Unsafe (US) output line. This line is connected to the fault detector, which will pass a write fault message to the PLA.

When the IC is in read mode, data is read from the selected head, amplified, and output on the differential DX, DY lines to the read chain amplifier and signal conditioner. If a fault condition exists such that write current is applied to the IC when it is in the read mode, the write current will be drawn from the Unsafe line and the fault will be detected by the fault detector.

3-68. SERVO HEAD. The servo head is a read only head constructed similarly to the read/write heads. The output of the head is amplified by a servo preamplifier IC mounted on the rotary arm of the actuator.

3-69. SERVO PREAMPLIFIER IC. The servo preamplifier IC is a 2-stage differential amplifier designed for use as a preamplifier for a magnetic servo head. The preamplifier output, labeled SERVO+, SERVO-, is connected to the input of the actuator servo control demodulator via the flexible printed-circuit cable used to connect the read preamplifier/write driver IC signal lines to the read/write data channel.

3-70. SPINDLE MOTOR. The spindle motor is a 3-phase brushless dc motor which spins the discs at a speed of 3,600 rpm. Incorporated in the motor are three Hall-effect sensors which are used by the spindle speed control circuit to indicate which of the three phases should be driven. A fourth Hall-effect sensor in the motor provides a start of track Index signal. Signal Index is used for timing purposes within A1 and is passed via an output buffer to the ST-506 Interface as Index signal INDX-L.

3-71. AIR FILTRATION COMPONENTS. A self-contained recirculating filter supplies clean air through a 0.3 micron filter to the sealed head-disc module. A separate filter allows for ambient pressure equalization within the sealed head-disc module without the introduction of contaminants.

3-72. ACTUATOR LOCK DRIVER

The actuator lock is controlled by a solenoid which is energized at power-on after the microprocessor detects that the spindle motor is up to speed (At Speed signal true). At this time, the microprocessor activates its Pick line which in turn causes the actuator lock driver to energize the lock solenoid. The actuator arm is now released, allowing the heads to move over the discs.

3-73. SPINDLE SPEED CONTROL

The three Hall-effect sensor outputs from the spindle motor are input to a ROM commutator in a solid-state spindle speed control circuit which decides which of the three outputs from the circuit should be driven to spin the motor in the proper direction. The speed of the motor is controlled by a phase-locked frequency regulator which compares a 360-Hz signal from the clock generator with the signals from the three Hall-effect sensors. This regulator circuit provides feedback to drivers in the speed control circuit such that the speed of the motor is maintained at 3,600 rpm, plus or minus 3.6 rpm.

At power-on, after the Power On Reset signal is turned off, the microprocessor sets the Stop Motor signal false, causing the spindle motor dynamic brake to activate. At the same time, the microprocessor disables the spindle speed control circuit by deactivating the Normal Regulation line. This allows the spindle motor to accelerate without any speed regulation. The microprocessor monitors the motor speed by measuring the time interval between the Index pulses from the spindle motor. When the time interval between the pulses indicates that the speed is within one percent of 3,600 rpm, the microprocessor enables the speed control circuit by activating the Normal Regulation line. The microprocessor stops the spindle motor by application of the Stop Motor signal to the spindle speed control and relay driver circuits.

3-74. SPINDLE SPEED CHECKER

The spindle speed checker circuit monitors the speed of the spindle motor by comparing the frequency of the Index pulses from the spindle motor hall-effect sensor with a 92.1-kHz clock signal from the clock generator. The microprocessor monitors the At Speed and Counter Not Ready outputs from the speed checker circuit and shuts down operation of the disc drive if the speed is determined to be outside of a predetermined range.

3-75. SPINDLE MOTOR BRAKE RELAY AND RELAY DRIVER

The spindle speed control circuit includes a dynamic brake which brings the spindle motor to a rapid halt when the microprocessor issues a Stop Motor signal. Signal Stop Motor activates the relay driver which in turn causes the spindle motor brake relay to connect low-value resistors across the winding of the spindle motor. At the same time, signal Stop Motor, input to the speed control circuit, disables the 3-phase drive to the motor.

3-76. ACTUATOR SERVO CONTROL

Actuator positioning and head track following is achieved on a closed-loop basis using a dedicated servo surface. The servo information is written on the bottom surface of the bottom disc. The servo system employs a dual-frequency technique based on an amplitude difference between alternating servo tracks written at two different frequencies. On track is realized for a data head when the servo head is positioned exactly between two servo tracks. In operation, a demodulator circuit continuously samples the two frequencies from the servo head, sums and averages the two signals, and produces a position error signal (PES). This PES signal is linearly proportional to the error (off track) amount and also indicates the off track direction.

During track following, the PES voltage is input to a transconductance power amplifier which supplies drive current to the actuator voice coil. This causes the actuator to hold the servo head at a point where the PES voltage is zero -- exactly between the two servo tracks. Since the servo head and the read/write heads are fixed on the rigid rotary arm of the actuator, any movement of the servo head is translated to all of the read/write heads.

Signal PES is also used during a seek operation. As the rotary arm is moving across the discs during a seek, the PES voltage is a series of positive and negative peaks which the microprocessor counts to determine track location. Also, the slope of the PES voltage is used to determine the velocity of the rotary arm during the seek operation.

The dual-frequency technique described above is relatively insensitive to servo surface medium defects. Also, servo head azimuth alignment is not a critical factor in the operation of the system.

The actuator servo control circuitry includes a demodulator, mode select switch, tachometer, digital-to-analog converter (DAC), and amplifier. Details of these circuits are provided in the following paragraphs.

3-77. DEMODULATOR. The Servo+, Servo- signal (read from the servo surface via the servo head and the servo preamplifier IC) consists of a combination of the frequencies recorded on alternate servo tracks -- 700 kHz and 1020 kHz. This signal is amplified and then separated into two frequencies by two identical mixer channels in the demodulator. In one channel, the 700 kHz is mixed with 576 kHz from the clock generator to produce 124 kHz. In the other channel, the 1020 kHz is mixed with 1152 kHz from the clock generator to produce 132 kHz. Higher frequencies are attenuated with active low-pass filters in the mixer channels. The two outputs from the mixer channels are rectified, averaged, and fed to the input of a difference amplifier. The output of this amplifier is Position Error Signal PES. When the servo head is positioned exactly between two servo tracks (read/write head on track), PES is zero. Displacement from this position (read/write head off track) cause PES to go either positive or negative, depending on the direction of offset and with an amplitude equal to the amount of the offset. A PES level of 1 volt equals a displacement of approximately 100 microinches.

The rectified and averaged outputs from the two mixer channels are also fed to a summing and AGC amplifier which supplies an AGC voltage to the amplifier at the input of the demodulator.

The demodulator also contains a track zero detector. This circuit senses the presence of a third frequency (1100 kHz) recorded on the servo surface to identify track zero. The Track 0 output from the detector is coupled to the microprocessor which in turn transmits Track Zero signal TRK0-L on the ST-506 Interface.

3-78. MODE SELECT SWITCH. The mode select switch is a solid-state circuit which places the actuator servo control circuitry in either a seek (velocity) or track follow mode of operation. Operation of the switch is controlled by the Seek signal from the microprocessor.

3-79. SEEK MODE. The seek mode of operation is selected by the microprocessor when it switches the mode select switch to the seek position with its Seek line. This selects a number of circuit blocks which together comprise a negative feedback servo control system supplying drive current to the actuator voice coil. These circuits include a velocity digital-to-analog converter (DAC), tachometer, slope selector, current inverter, on-peak detector, inverter, and power amplifier.

3-80. Velocity DAC. The velocity DAC is a standard integrated-circuit digital-to-analog converter which outputs a velocity error dc voltage to the servo system in response to an 8-bit velocity error command from the microprocessor.

3-81. Tachometer. The tachometer provides a measurement of the actuator velocity by integrating the slope of the PES signal as the actuator crosses tracks. However, the PES voltage becomes non-linear at the peaks of its triangle-shaped waveform. Therefore, at this time the power amplifier current to the actuator voice coil is differentiated to provide an indication of actuator velocity.

3-82. Slope Selector. The slope selector circuit, programmed by the Even In signal from the microprocessor, selects a PES slope of the proper polarity for the tachometer to provide a negative feedback.

3-83. Current Inverter. The current inverter, with a gain of plus or minus one and programmed with the Odd In signal from the microprocessor, selects a current of the proper polarity from the power amplifier for input to the tachometer.

3-84. On-Peak Detector. The on-peak detector operates at approximately 3.5 volts to initiate the switch between the integrated PES signal and the differentiated motor current in the tachometer. The output of the on-peak detector is also coupled to the microprocessor to signal track crossings.

3-85. Power Amplifier. The power amplifier is a transconductance amplifier which supplies current to the actuator voice coil in response to an error voltage input. The amplifier output lines are labeled VCMA, VCMB. The amplifier is enabled by the Servo Enable line from the microprocessor.

3-86. Inverter. The inverter has a gain of plus or minus one and is programmed with signal Odd In from the microprocessor. The purpose of the inverter is to select an error voltage of the correct polarity for input to the power amplifier. The input to the inverter is from the tachometer (seek mode) or signal PES (track follow mode), as selected by the mode select switch.

3-87. TRACK-FOLLOW MODE. The track-follow mode of operation is selected by the microprocessor at the end of a seek operation when the addressed track has been reached. Signal PES is applied via the track-follow position of the mode select switch through the inverter to the input of the power amplifier. Signal Odd In from the microprocessor programs the inverter to select a PES voltage of the proper polarity to provide a negative feedback signal to the amplifier.

3-88. OFF-TRACK DETECTOR. The off-track detector monitors the amplitude of the PES signal and provides an Off Track output to the microprocessor whenever the PES voltage exceeds plus or minus 1.5 volts.

3-89. SEEK OPERATION. The disc drive must have Ready RDY-L and Seek Complete SKCMP-L true before a seek operation can begin. With the disc drive in this state, the microprocessor is in its basic loop, monitoring Motor Speed, Off Track, and looking for either a Step STEP-L pulse or Write Gate WGATE-L, both of which are gated by Drive Select DS0-L. When a Step pulse is received, the Step signal forces Seek Complete SKCMP-L false. If Write Gate is true and Seek Complete goes false, a fault condition will be issued, automatically deactivating the write circuitry. When a Step pulse is received and Write Gate in not true, then the microprocessor will initiate a seek operation. The microprocessor will set the direction of the seek from the information on the Direction DIR-L line. The microprocessor will also set the seek mode, at which time the actuator servo control circuit will cause the actuator to move. The speed at which the actuator moves is dependent on the rate at which the Step pulses are received. Maximum performance of the actuator is attained if the time interval between Step pulses is less than 39 microseconds.

The microprocessor counts the track crossings until there are no more Step pulses and the actuator is crossing the last track. At this time, the microprocessor switches the actuator servo control from the seek mode to the track follow mode. The microprocessor now starts a settling timer and looks for an off-track condition. If an off-track condition exists, the microprocessor restarts the settling timer. This is done until the off-track condition is cleared plus the settling time. Once this is accomplished, the microprocessor sets Seek Complete line SKCMP-L.

3-90. RESTORE TO TRACK 0 OPERATION. To perform a restore to track 0 operation, the microprocessor enables the actuator servo control circuit and moves the actuator over the data area and out of the landing zone into the outer guard band area. Once the microprocessor detects that the actuator is in the outer guard band area, the microprocessor will cause the actuator servo control circuit to settle the actuator on a data track. The microprocessor will set direction out with a slow velocity, and count the track crossings until the track zero signal is detected. The microprocessor will now cause the servo control circuit to lock onto a track and check for the track 0 signal. After the servo control circuit is locked onto track

0, the microprocessor will initiate its maximum and minimum track counter. When this is accomplished, the microprocessor will activate Drive Ready signal RDY-L and Seek Complete signal SKCMP-L.

3-91. READ/WRITE DATA CHANNEL

The read/write data channel includes head select and control logic, a read chain which amplifies and qualifies the differential MFM-encoded read signal from the read preamplifier/write driver IC's in the sealed head-disc module, and a write channel which converts the TTL-level MFM-encoded write data signal from DDC PCA-A2 into write current drive for the read preamplifier/write driver IC's.

3-92. HEAD SELECT AND CONTROL LOGIC

The head select and control logic block performs a hardware decode of ST-506 Head Select signals HS0-L through HS4-L and the Write Gate signal from the PLA. (Head Select line HS8-L is not used in the HP 7941 and HP 7945.) The output signals from the block enable the write driver/read preamplifier IC, select one of four read/write heads, and activate the read function or write function. The output lines are labeled Chip Enable CE0-L, CE1-L; binary Head Select bits HS1-H, HS2-H; and Write Enable WS. In the HP 7945, where two IC's are used to control seven heads, Chip Enable CE0-L selects one IC for controlling heads 0 through 3, and CE1-L selects the other IC for controlling heads 4 through 6. Signals HS1-L, HS2-H, and WS are input to both IC's.

3-93. READ CHAIN. The read chain receives differential current DX, DY from the read preamplifier portion of the read preamplifier/write driver IC's. This signal represents magnetic transitions seen by the head as it flies over the magnetic recording medium. Whenever the head passes over a magnetic transition, the preamplifier differential output peaks. The read chain amplifies this differential analog signal and converts it to a stream of differential logic-level pulses, one for every signal peak. These MFM-encoded pulses are sent to the DDC for decoding. The read chain circuitry includes an amplifier/signal conditioner stage and a differential line driver.

3-94. Amplifier/Signal Conditioner. In the amplifier section of the block, the differential DX, DY input is amplified, filtered and subjected to automatic gain control (AGC). A diode matrix at the input of the amplifier, controlled by the Write Enable signal from the microprocessor, isolates the read chain from the write chain during a write operation. The AGC circuit compensates for signal variations caused by normal differences in head flying height, head characteristics, and recording medium. The AGC circuit includes an AGC hold feature which maintains AGC control when switching between heads. Following AGC, the signal is filtered, differentiated, and input to a zero-crossing detector which converts the differential analog signals into logic-level pulses.

Circuitry in the signal conditioner portion of the block prevents noise in the analog input signal from producing false zero crossings. This is achieved by applying the output of the zero-crossing detector to a gating circuit which effectively screens out spurious pulses caused by noise.

3-95. Differential Line Driver. The conditioned output signal is coupled via a differential line driver to the ST-506 Interface. The output lines from the line driver are labeled RMFM+, RMFM-.

3-96. WRITE CHAIN. The write chain receives differential MFM-encoded write data from the DDC and converts the data to a differential signal suitable for transmission to the write driver section of the read preamplifier/write driver IC's. The write chain circuitry includes a line receiver, a transition generator, a write current source, and a write fault detector.

3-97. Line Receiver. The line receiver translates the differential MFM-encoded write data on the ST-506 Interface WMFM+, WMFM- lines into a single-ended format suitable for input to the transition generator. The output of the line receiver is a positive-going pulse for every magnetic transition to be written on the disc.

3-98. Transition Generator. The transition generator divides the MFM frequency by two so that the logic level of the output determines the direction of current through the head. Each transition in MFM generates a transition on the recording medium.

3-99. Write Current Source. The write current source provides current for the read/write heads and supplies a write control (WC) signal to the read preamplifier/write driver IC's. The write current source is enabled by the Write Gate line from the microprocessor and has two outputs, selected by the Inner Track line. For tracks 0 to 511, the write current output is 27.5 milliamperes and for tracks 512 and above, the write current is 22.5 milliamperes.

3-100. Write Fault Detector. During a write operation, the microprocessor monitors certain key parameters of the operation via the write fault detector. If an abnormal condition is detected, the microprocessor activates, via the PLA, Write Fault signal WFLT-L. Inputs to the write fault detector include Unsafe signal US from the write driver/read preamplifier IC, and lines from the write current source and the head select logic. The faults which can cause WFLT-L to become active are listed in table 3-1 under the description for signal WFLT-L.

3-101. SELF TEST

Disc drive assembly A1 performs a self-test of certain key hardware functions at power-on. These functions include head loading and seeking to track 0. Following successful completion of the tests, Ready RDY-L and Seek Complete SKCMP-L are set true, allowing A1 to respond to DDC commands via the ST-506 Interface. During normal operation of the disc drive, the microprocessor monitors spindle speed and off-track conditions. If either parameter exceeds predetermined limits, the microprocessor shuts down operation via the RDY-L and SKCMP-L lines.

3-102. POWER-ON RESET

The power-on reset circuit monitors the +5, +12, and -10 voltages in the disc drive. (The +5 and +12 voltages are input from power supply assembly A4 and the -10 volt supply is generated internally in disc drive assembly A1.) At power on, the Power On Reset output signal is active, holding the electronics in disc drive assembly A1 in a reset condition until the voltages reach their proper levels. During operation of the disc drive, if any one of the voltages falls below a predetermined level, Power On Reset will become active and shut down operation of the disc drive.

3-103. POWER SUPPLY A4

Power supply assembly A4 develops dc operating voltages from the ac line voltage and distributes these voltages throughout the disc drive. The power supply assembly also generates a power-on reset signal.

Power supply assembly A4 is a self-contained switch-mode power supply mounted on a printed-circuit assembly. See sheet 1A . Located in the assembly are all of the ac line voltage components including the line cord connector, line fuse, line voltage selector switch, line on/off switch, and line filter. Output voltages are +5 Vdc, +12 Vdc, and -12 Vdc. (The -12 Vdc output is not used in the HP 7941 and HP 7945 Disc Drives.) The power supply output voltages and power-on reset signal can be measured at test points at the front of PCA-A4. See figure 4-8. The output voltages are not adjustable. The power supply voltages are connected to host dependent controller PCA-A5, device dependent controller PCA-A2, and disc drive assembly A1 via cable assembly W1.

The following paragraphs provide a more detailed description of the power supply A4 circuitry, as shown in sheet 1A . Refer to table 3-1 for a description of the mnemonics used in sheet 1A and to figure 4-10 for detailed voltage and signal distribution information.

3-104. AC INPUT CIRCUITS

The ac line voltage is connected to power supply assembly A4 through a printed-circuit assembly (PCA) mounted ~AC LINE connector. A PCA-mounted ac line on/off switch controls both sides of the ac line into the power supply. The switch is operated by a LINE~ pushbutton projecting through an opening on the front panel of the disc drive. There is a fuse in the line side of the ac input following the power switch. The fuse value is the same (3A, 250V) for both 115-Vac and 230-Vac inputs. A line filter following the fuse reduces the level of line transients entering the power supply and the amount of switching noise leaving the power supply.

Also associated with the input circuitry is a VOLTAGE SELECTOR switch which selects line voltages of 115 Vac or 230 Vac. When the switch is in the 115 Vac position, a surge voltage

protection device protects the power supply from damage if it is inadvertently connected to 230 Vac.

3-105. SWITCH-MODE SUPPLY

The switch-mode supply consists basically of an ac-dc converter and a flyback-mode dc-dc converter. The ac-dc converter rectifies and filters the ac line voltage. This filtered dc operating voltage is supplied to the dc-dc converter. Included in the ac-dc converter are two thermistors that limit the initial power on surge current to approximately 25 amperes peak at 115 Vac and 230 Vac. The dc-dc converter chops the dc input into time-varying voltages, transforms them to lower levels and filters the outputs to supply the desired dc voltages of +5, +12, and -12 Vdc.

3-106. POWER-ON RESET

The power-on reset circuit is activated by the +5V output from power supply assembly A4 and produces Power Valid signal PVAL-H. At power on, PVAL-H remains low for at least 100 milliseconds after the +5V output reaches 4.75V or higher. Signal PVAL-H then goes to a high level. Signal PVAL-H will also go low for at least 500 microseconds prior to the +5V going below 4.75V. Signal PVAL-H can be monitored at a test point on the front of power supply PCA-A4. See figure 4-8. PVAL-H is connected to device dependent controller PCA-A2.

Table 3-1. List of Mnemonics

MNEMONIC	SIGNAL	SOURCE	DESCRIPTION
ATN-L	Attention	A5 1A	HP-IB management interface line used to specify how information on bidirectional Data I/O Bus DIO1-L through DIO8-L is to be interpreted and which device must respond to the information. When ATN-L is low , the DIO1-H through DIO8-H lines carry addresses or commands. When ATN-L is high, the DIO1-H through DIO8-H lines carry data.
CE0-L, CE1-L	Chip Enable, Bits 0,1	A1 1C	Enable the read preamplifier/write driver IC in the head-disc module of disc drive assembly A1.
CSA0-H thru CSA5-H	Control/Status Address Bus, Bits 0 thru 5	A5 1A	DC-IB signals used to access the registers in a selected DDC which comprise the Control/Status Data Bus CSB0-H through CSB7-H. Output to DDC PCA-A2 1B via cable W2.
CSB0-H thru CSB7-H	Control/Status Data Bus, Bits 0 thru 7	A5/A2 1A / 1B	DC-IB bidirectional 8-bit bus used to pass control and status data between the HDC and a selected DDC. Output to DDC PCA A2 1B via cable W2.
CSRS-L	Control/Status Read Strobe	A5 1A	DC-IB signal used to pass bytes from the DDC to the HDC over Control/Status Data Bus CSB0-H through CSB7-H. The bytes are of a DDC-status nature since recording medium information is passed over Read/Write Data Bus DATA0-H through DATA7-H. The read strobe generates a 500-nanosecond control/status bus read cycle. Output to DDC PCA-A2 1B via cable W2.
CSWS-L	Control/Status Write Strobe	A5 1A	DC-IB signal used to pass control bytes from the HDC to the DDC over Control/Status Data Bus CSB0-H through CSB7-H. Output to DDC A2 1B via cable W2.

Table 3-1. List of Mnemonics (Continued)

MNEMONIC	SIGNAL	SOURCE	DESCRIPTION
DATA0-H thru DATA7-H	Read/Write Data Bus, Bits 0 thru 7	A5/A2 1A/1B	DC-IB bidirectional 8-bit bus used to pass read/write data between the HDC and a selected DDC or vice versa. Connected between HDC PCA-A5 1A and DDC PCA-A2 1B via cable W2.
DAV-L	Data Valid	A5 1A	HP-IB handshake line used to indicate availability and validity of information on Data I/O Bus DIO1-L through DIO8-L. DAV-L indicates to a receiving device that data is available.
DIO1-L thru DIO8-L	HP-IB Data I/O Bus, Bits 1 thru 8	A5 1A	HP-IB bidirectional data input/output (I/O) bus used for the transfer of data, commands, and other messages between the host computer and the HDC. Transfer is bit parallel, byte serial.
DIR-L	Direction	A2 1B	ST-506 Interface control signal. DIR-L defines the direction of motion of the read/write heads when Step signal STEP-L is pulsed. An inactive (high) DIR-L defines an "out" direction and when STEP-L is pulsed, the read/write heads move away from the center of the disc. Conversely, an active (low) DIR-L defines an "in" direction and the read/write heads move towards the center of the disc. Output to disc drive assembly A1 1C via cable W3.
DRIN-L/ DROUT-L	Data Request In/ Data Request Out	A2 1B	DC-IB tri-state DMA request lines used to transfer bytes over Read/Write Data Bus DATA0-H through DATA7-H. The "out" direction is defined as being from the HDC to the DDC. A DDC is programmed via Control/Status Data Bus CSB0-H through CSB7-H to drive a given request line. Output to HDC PCA-A5 1A via cable W2.

Table 3-1. List of Mnemonics (Continued)

MNEMONIC	SIGNAL	SOURCE	DESCRIPTION
DS0-L	Drive Select, bit 0	A2 1B	When active (low), connects the ST-506 Interface control lines to disc drive assembly A1 interface circuitry. Output to disc drive assembly A1 1C via cable W3.
DSIN-L/ DSOUT-L	Data Strobe In/ Data Strobe Out	A5 1A	DC-IB HDC-generated strobe lines which accomplish the transferring of data between the the HDC and one or two DDC's over Read/Write Data Bus DATA0-H through DATA7-H.
DX, DY	Differential Data	A1 1C	Differential signal lines to/from read preamplifier/write driver IC's.
EOI-L	End Or Identify	A5 1A	HP-IB control signal used to indicate the end of multiple byte transfers or used with signal ATN-L to perform a parallel polling sequence.
GREEN-L	Green	A2 1B	Drive for green LED in front panel FAULT/ON LINE indicator. Output to the front panel via cable W4.
HS0-L, HS1-L, HS4-L, HS8-L	Head Select, Bits 0 thru 8	A2 1B	ST-506 Interface control signals. These lines provide a means of selecting each individual read/write head in a binary-coded fashion. When all four lines are inactive, head 0 is selected. Output to disc drive assembly A1 1C via cable W3.
HS1-H, HS2-H	Head Select, Bits 1, 2	A1 1C	Head select bits input to read preamp/write driver IC's from the head select and control logic.
IFC-L	Interface Clear	A5 1A	HP-IB general management line used to place the interface system in a known quiescent state.
INDX-L	Index	A1 1C	ST-506 Interface control line. INDX-L is provided by disc drive assembly A1 once each revolution of the disc (16.67 milliseconds nominal) to indicate the beginning of a track.

Table 3-1. List of Mnemonics (Continued)

MNEMONIC	SIGNAL	SOURCE	DESCRIPTION
			Normally, the signal is a high level and the transition to a low level indicates the start of a track. The signal is generated by a Hall-effect sensor in the spindle motor. Output to DDC PCA-A2 1B via cable W3.
NDAC-L	Not Data Accepted	A5 1A	HP-IB handshake line used to indicate the acceptance of data by all devices.
NRFD-L	Not Ready For Data	A5 1A	HP-IB handshake line used to indicate that all devices are, or are not, ready to accept data over Data I/O Bus DIO1-H through DIO8-H.
PES	Position Error Signal	A1 1C	Actuator servo control circuit signal indicating amount and direction of head off-track displacement.
PVAL-H	Power Valid	A4 1A	Indicates that power supply A4 outputs are up to their proper values. Output to DDC PCA-A2 1B via cable W1.
RDY-L	Ready	A1 1C	ST-506 Interface control signal. RDY-L becomes active (low) following power on if a) dc voltages are within specification, b) discs are at speed, and c) head position is recalibrated. Output to DDC PCA-A2 1B via cable W2. If there is a fault in the dc voltages or spindle speed control, RDY-L will remain inactive (high). RDY-L will not go low until the fault is cleared and the head position is recalibrated. After power on, RDY-L should become active within 25 seconds. During operation of the disc drive, the processor is continually monitoring the speed of the spindle motor. If a speed variation of greater than 2 percent is detected, the processor will force RDY-L high, lock the actuator, and stop the motor. Power on recycling is required to restart the disc drive.

Table 3-1. List of Mnemonics (Continued)

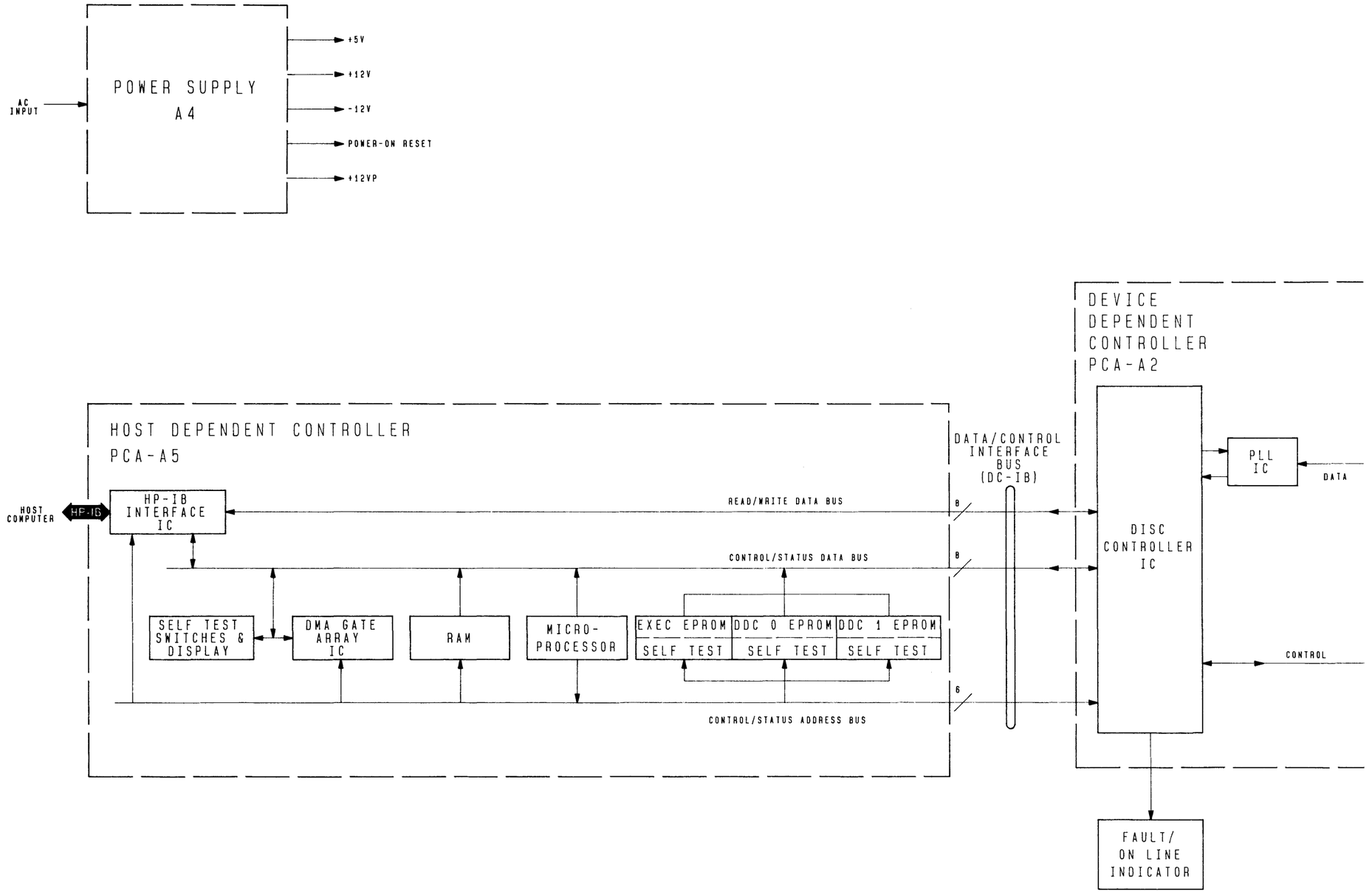
MNEMONIC	SIGNAL	SOURCE	DESCRIPTION
RED-L	Red	A2 1B	Drive for red LED in front panel FAULT/ON LINE indicator. Output to the front panel via cable W4.
REN-L	Remote Enable	A5 1A	HP-IB control line used in conjunction with other messages to select between two alternate sources of device programming data.
RMFM+, RMFM-	MFM Read Data	A1 1C	ST-506 Interface data signal. A differential signal which defines the MFM transitions recovered by reading a prerecorded track with a selected head. The transition of the RMFM+ line going more positive than the RMFM-line represents a flux reversal on the track. Output to DDC PCA-A2 1B via cable W4.
SEL-L	Select	A5 1A	DC-IB signal used to select which DDC will respond to a given control/status bus operation. When low, SEL-L selects DDC 0 (disc drive.)
SKCMP-L	Seek Complete	A1 1C	ST-506 Interface control signal. SKCMP-L indicates that the read/write heads have settled on the final track at the end of a seek operation. Reading or writing should not be attempted when SKCMP-L is inactive (high). Output to DDC PCA-A2 1B via cable W3.
SRQ-L	Service Request	A5 1A	HP-IB general management line. SRQ-L is used by a device to indicate the need for service and to request an interrupt of the current activity.
STEP-L	Step	A2 1B	ST-506 Interface control signal. STEP-L causes the read/write heads to move in the direction of motion defined by Direction signal DIR-L. One Step pulse = one step = one track. Output to disc drive assembly A1 1C via cable W3.
TRK0-L	Track 0	A1 1C	Indicates when the read/write heads are positioned at cylinder 0 (the outermost data track). Output to DDC PCA-A2 1B via cable W3.

Table 3-1. List of Mnemonics (Continued)

MNEMONIC	SIGNAL	SOURCE	DESCRIPTION
US	Unsafe Current	A1 1C	A read preamplifier/write driver line in which current flows whenever writing is enabled and there is an absence of write current or data transitions.
VCMA, VCMB	Actuator Voice Coil Drive	1A 1C	Drive current to actuator voice coil. Signal is supplied by actuator servo control circuit.
WC	Write Current	1A 1C	A line from the write current source sending current to the read read/write head during a write. Output to the read preamplifier/ write driver IC's.
WFLT-L	Write Fault	A1 1C	ST-506 Interface control signal. WFLT-L warns that a condition exists in disc drive assembly A1 which makes writing unsafe. Output to DDC PCA-A2 1B via cable W3. Signal becomes active for the following reasons. WRITING: • Open head. • Shorted head. • Improper write current. • An offtrack condition occurs. • Invalid or multiple heads are selected. • Spindle speed loss when writing. • A write is attempted when SKCMP-L is inactive (high). • Write gate but no write data. • Attempting to write with RDY-L inactive (high). • A write attempted when the disc drive is write protected with the write protect option. READING: • Write current appears at head. Disc drive assembly A1 will not accept further commands after a write fault has been detected by the microprocessor.

Table 3-1. List of Mnemonics (Continued)

MNEMONIC	SIGNAL	SOURCE	DESCRIPTION
			If the disc drive is deselected, the microprocessor will reexamine the fault and reactivate itself if the condition clears.
WGATE-L	Write Gate	A2 1B	ST-506 Interface control signal. When WGATE-L is active (low), it enables write data to be written on the disc. When inactive (high), it enables data to be read from the disc. Output to disc drive assembly A1 1C via cable W3.
WMFM+, WMFM-	MFM Write Data	A2 1B	ST-506 Interface data signal. A differential MFM signal which defines the transitions to be written on a track. The transition of the WMFM+ line going more positive than the WMFM-line will cause a flux reversal on a track (provided that Write Gate WGATE-L is active). Output to disc drive assembly A1 1C via cable W3.
WS	Write Select	A1 1C	Selects the read or write mode of operation for the preamplifier/write driver IC's in the head-disc module. When WS is high, the write mode is selected; when WS is low, the read mode is selected.



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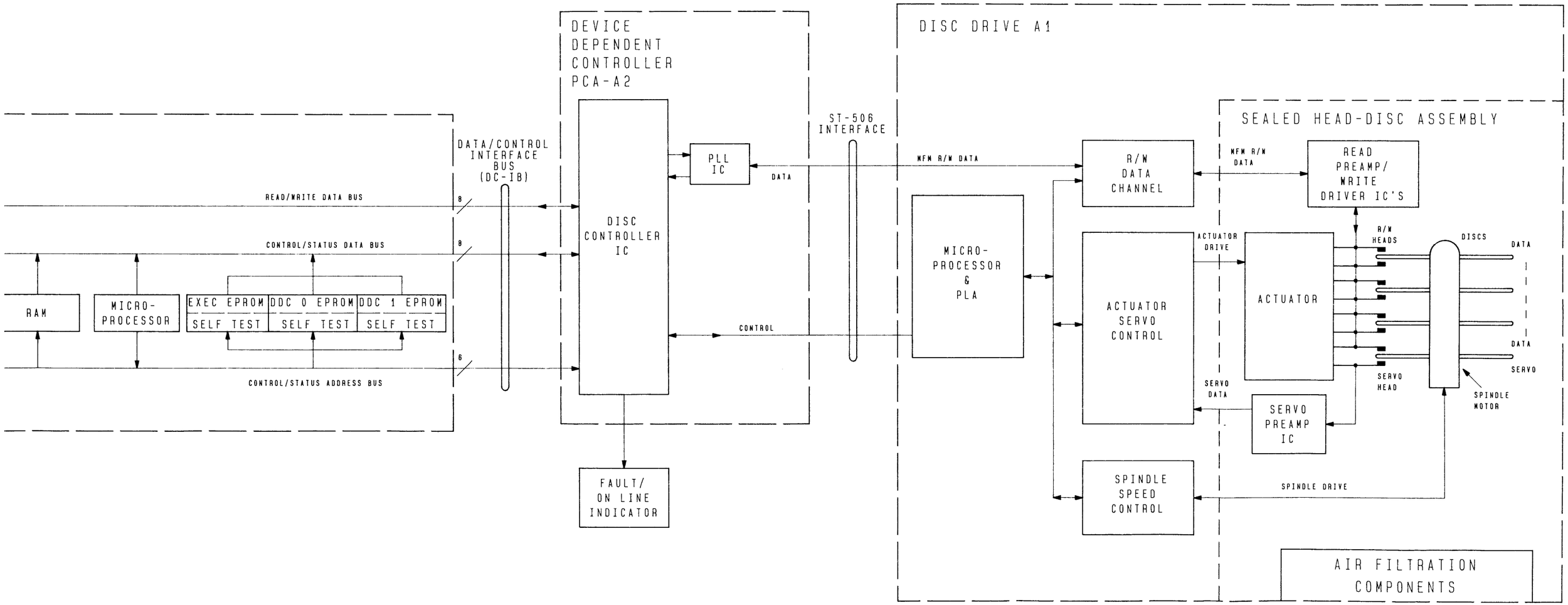


Figure 3-3. Disc Drive, Block Diagram

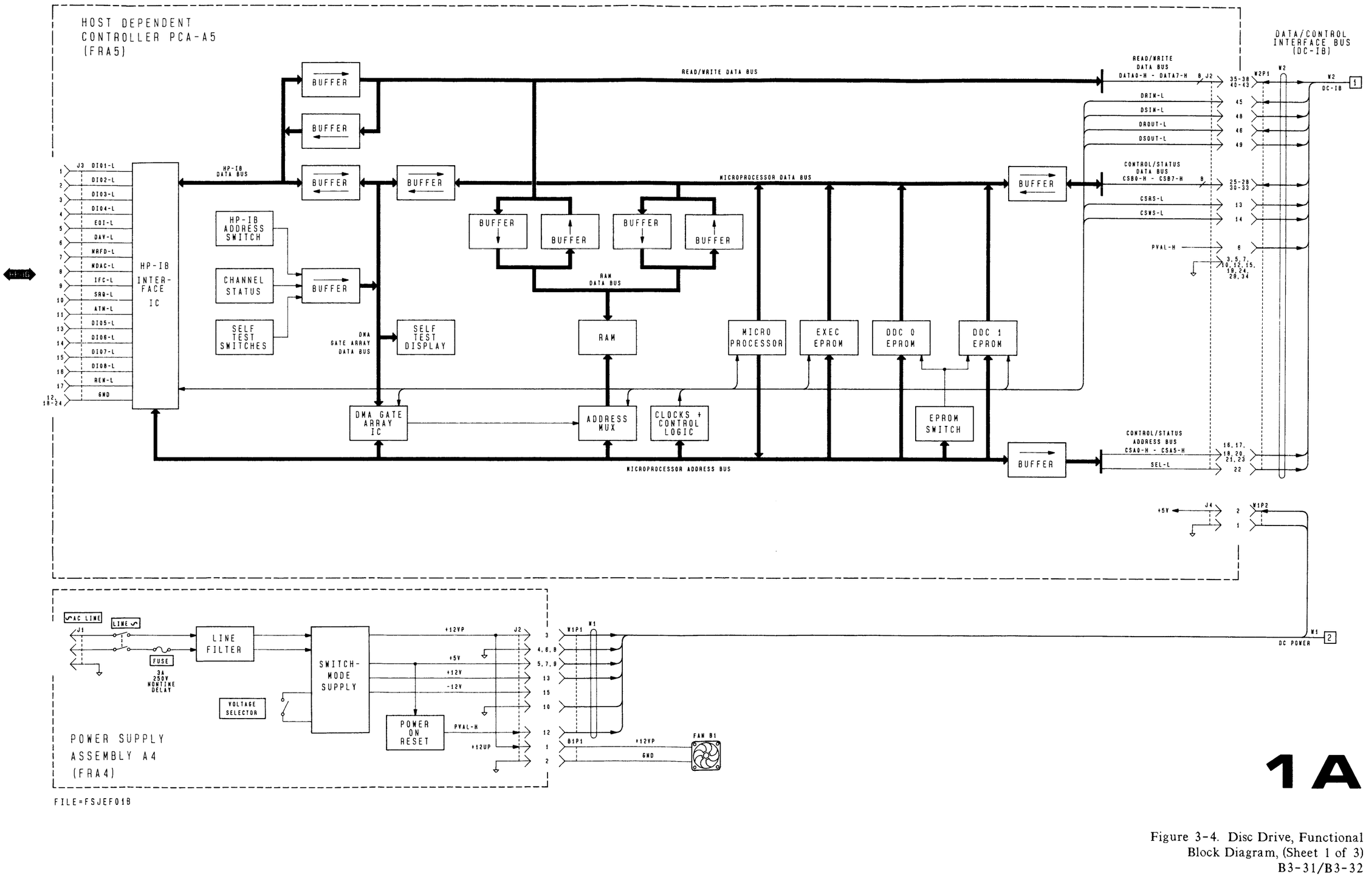
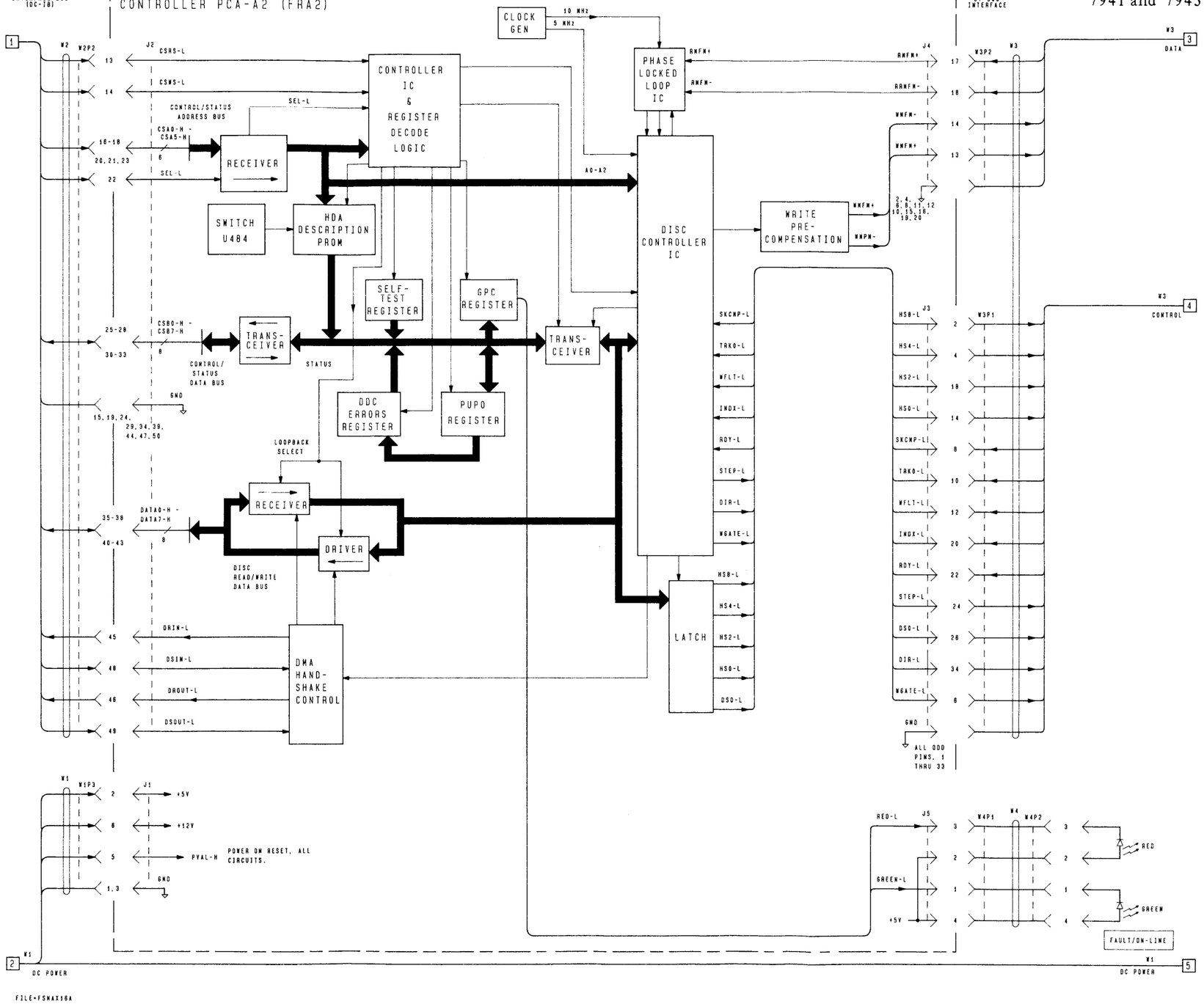
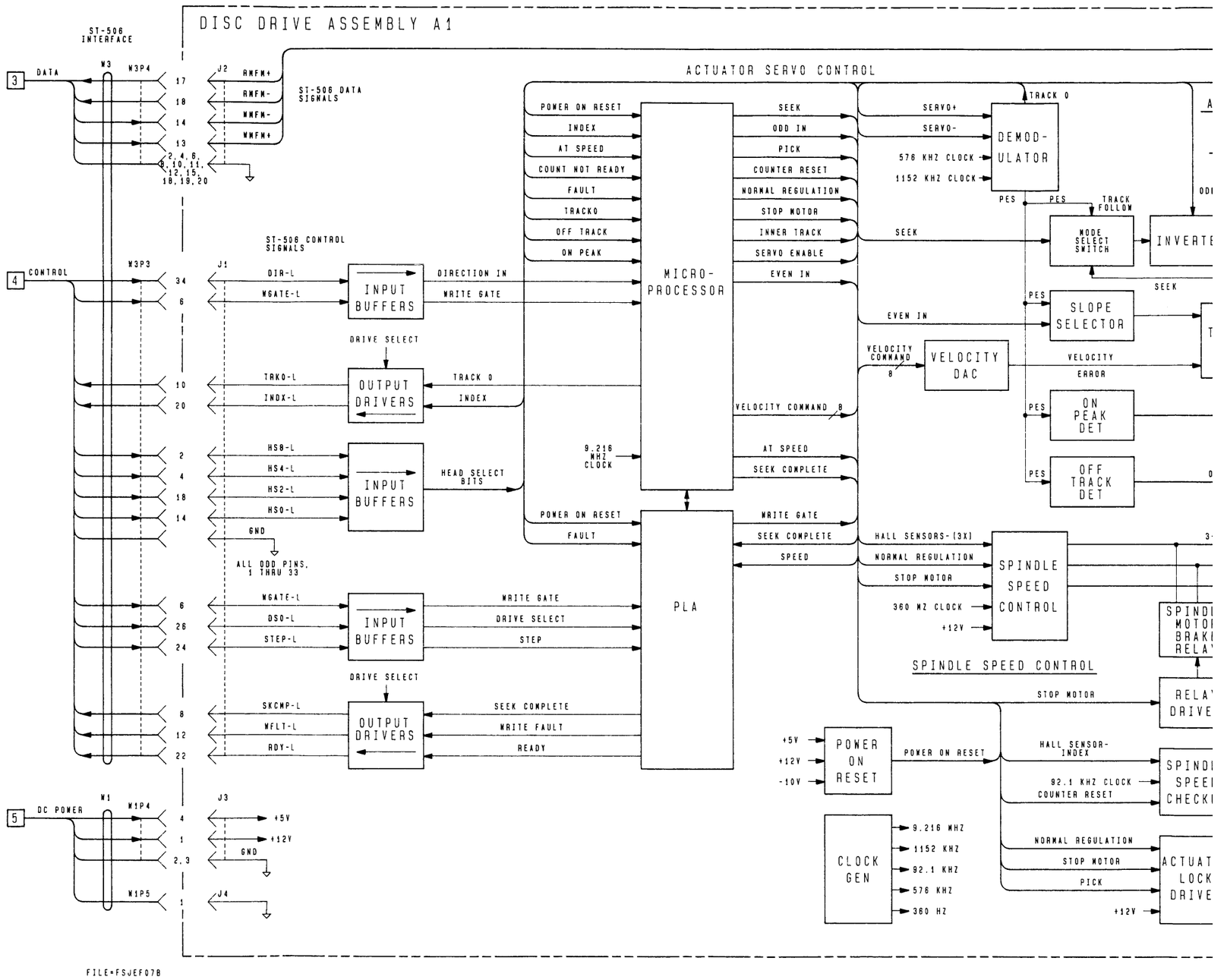


Figure 3-4. Disc Drive, Functional Block Diagram, (Sheet 1 of 3)

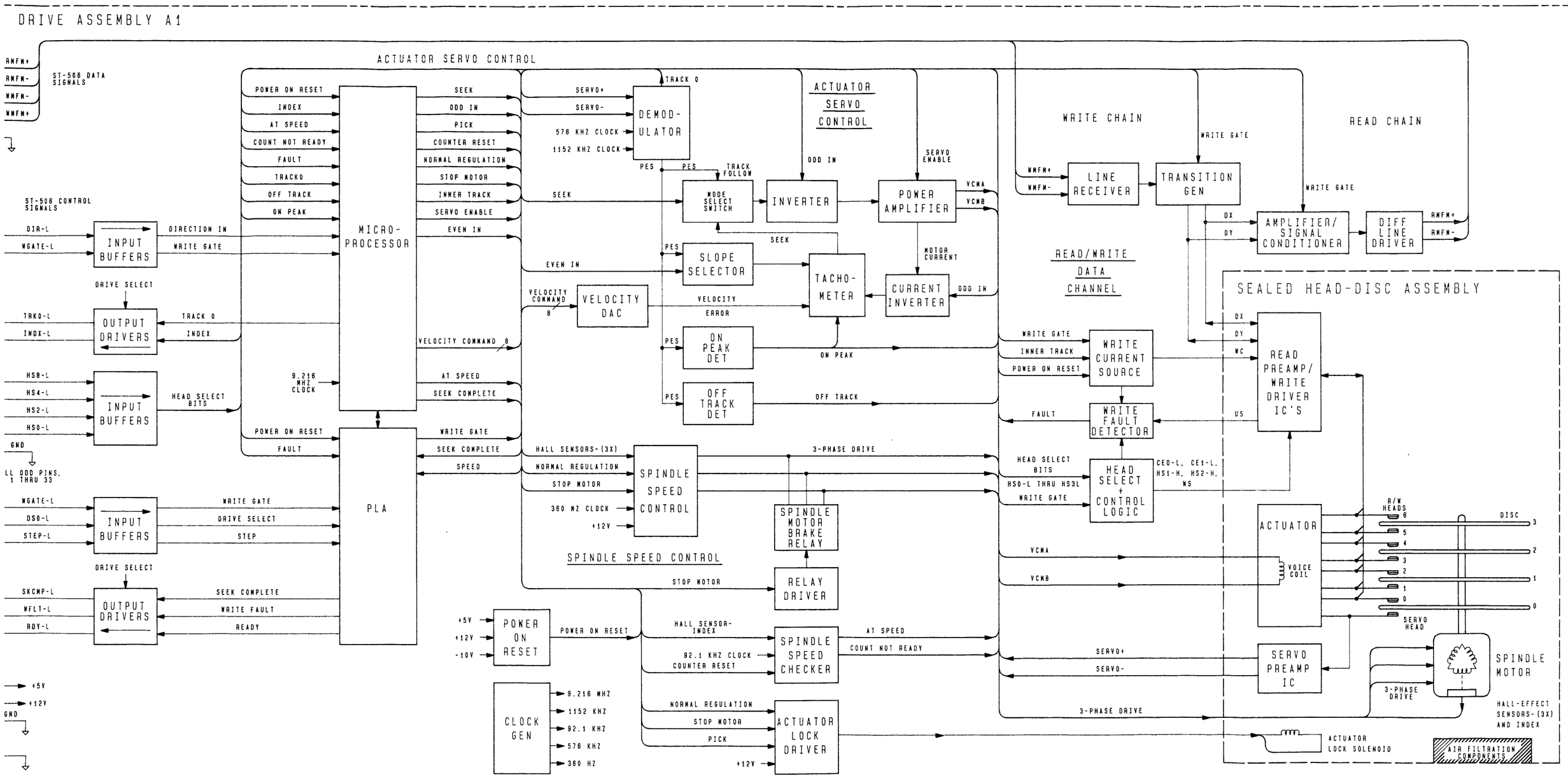


1B

Figure 3-4. Disc Drive, Functional Block Diagram, (Sheet 2 of 3)
B3-33/B3-34



FILE=FSJEF07B



1C

Figure 3-4. Disc Drive, Functional Block Diagram, (Sheet 3 of 3)
B3-35/B3-36

SERVICE INFORMATION

4-1. INTRODUCTION

WARNING

The disc drive does not contain operator serviceable parts. To prevent electrical shock, refer all service activities to service-trained personnel.

CAUTION

- The field replaceable assemblies (FRA's) in the disc drive are electrostatic sensitive devices. Take appropriate precautions when removing the FRA's from the disc drive. Use of an anti-static pad and wrist strap is required. (These components are contained in anti-static work station, part no. 9300-0749.) Immediately after removal, store the FRA's in anti-static, conductive plastic bags.

- The disc drive is delicate and should be handled with care. Also, the disc drive is heavier (9.9 kilograms/21.8 pounds) than its size would indicate.

- Do not turn the LINE~ switch on or off when the system is transferring data on the Hewlett-Packard Interface Bus (HP-IB).

- Do not cycle the LINE~ switch on and off unnecessarily.

- Do not connect or disconnect the HP-IB cable(s) from the disc drive when the system is transferring data on the HP-IB.

This section contains information useful for troubleshooting the disc drive. This information includes a description of the disc drive self-test and internal diagnostic routines, troubleshooting hints, and details of signal connections and power distribution.

4-2. SERVICE TOOLS

The following tools and materials are required to service the disc drive:

- Torx* T10 Driver
- Torx* T15 Driver
- Torx* T25 Driver
- Nut Driver, 9/32"
- Pozi Driver, No. 1
- Anti-Static Work Station, part no. 9300-0794

4-3. FRA LOCATIONS

The locations of the four field replaceable assemblies (FRA's) identified by the self-test diagnostics are shown in figure 4-3, Field Replaceable Assembly (FRA) Locations. Refer to section V for FRA removal and replacement instructions and to section VI for FRA identification and ordering information.

4-4. CABLE CONNECTORS

Figures 4-4 through 4-7 show the locations of the cable connectors on the four FRA's in the disc drive and the cables coupled to these connectors. Figure 6-1, Disc Drive, Exploded View, shows how the cables are connected between the FRA's. An overall cabling diagram of the disc drive is provided in figure 4-9, Cabling Diagram.

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4-5. SIGNAL DISTRIBUTION

Cable connections between the FRA's in the disc drive are shown in figure 4-9. The distribution of signals via these cables is shown in figure 4-10, Signal Distribution. The mnemonics appearing in figure 4-10 are defined in table 3-1, List of Mnemonics.

4-6. POWER DISTRIBUTION

Details of ac input wiring and dc power distribution are shown in figure 3-4, Disc Drive, Functional Block Diagram, Sheet 1, and in figure 4-9, Cabling Diagram.

4-7. SIGNAL NOTATION

In the disc drive logic circuits, a digital signal is applied to its destination in one of two states: active or inactive. The signal is active when its voltage level (high or low) makes the action occur for which the signal was designed. This action is usually identified by a signal mnemonic. Refer to table 3-1, List of Mnemonics. A mnemonic with an "-L" suffix indicates a logic signal with an active low voltage level. A mnemonic with an "-H" suffix indicates a logic signal with an active high voltage level. Signal mnemonics without an "-L" or "-H" suffix usually indicate analog, data bus, or control bus signals.

4-8. BLOCK DIAGRAM

A functional block diagram of the disc drive is provided in section III of this manual. (See figure 3-4.) To facilitate references to the three sheets of this diagram, each sheet is identified by a large bold numeral in the lower right-hand corner of the page. These numerals are boxed in text and table references, for example: 1A . Included in figure 3-4 are diagrams for host dependent controller FRA5 1A , device dependent controller FRA2 1B , disc drive assembly FRA1 1C , and power supply assembly FRA4 1A . Each of these diagrams in section III is accompanied by a circuit description.

4-9. TEST POINTS

A number of test points are provided in power supply FRA4 for troubleshooting and test purposes. The location of these test points is shown in figure 4-8, FRA4 (Power Supply A4), Test Points and Voltages. Also provided are specifications for the voltages monitored at the test points. The output voltages are not adjustable. It should be noted that access to the test points requires the removal of the front panel assembly from the disc drive. Refer to Section V for removal details.

4-10. SELF-TEST CONTROLS

The disc drive self-test controls include a red/green FAULT/ON LINE indicator on the front panel, together with two switches and a 2-digit hexadecimal Self-Test display on the rear panel. See figure 4-1, Self-Test Controls and Readout. Information regarding the use of these controls and indicators is provided in the following paragraphs.

4-11. FAULT/ON LINE INDICATOR

The FAULT/ON LINE indicator is a red/green display which signals the operating status of the disc drive. When line voltage is applied to the disc drive, the FAULT (red) and ON LINE (green) portions of the display will illuminate for one second to verify that the display is functioning. Next, the green portion will flash during the time that the disc drive is executing its internal self-test routines. Self test takes between six and twelve seconds to complete. If the disc drive passes self test, the display will change to a solid green. If the disc drive fails self test, the display will change to a solid red with a flashing green indicating that the self test failure has occurred, but that the self test routines are still accomplishing some "housekeeping" tasks. When these tasks are complete, the green indicator will extinguish, indicating that the disc drive is ready to accept host commands such as diagnostics. The green indicator will flash again when the disc drive attempts to respond to these commands. A solid red and green display indicates that the host dependent controller has failed self test.

After a successful self test, a solid green display indicates that the disc drive is idle and a flashing green display indicates that the disc drive is active.

4-12. SELF TEST SWITCH

The SELF TEST switch is a momentary contact pushbutton switch which initiates the disc drive internal self-test diagnostic routines. The switch is recessed behind the rear panel and can be activated by the tip of a ball point pen or similar object. The self-test routines initiated by the switch are the same as those initiated by a host-issued diagnostic command. Both of these routines are similar to the power on self-test routines except that certain host dependent controller (unit 2) subtests are not executed as these subtests would destroy the current runtime environment.

4-13. SELF-TEST DISPLAY

The Self-Test display consists of a 2-digit 7-segment hexadecimal display which reports the results of the internal self-test and diagnostic routines. Whenever self test is initiated, either by operation of the SELF TEST switch or when line voltage is applied, the display will first show a **8.8.** readout to indicate that all segments of the display are functioning. The display will then go blank until self test is completed. In the case of a self-test command issued by the system to unit 0, the display will immediately go blank (**8.8** is not displayed) and remain blank until self test is completed.

When the SELF TEST switch is pressed, release from the host is requested. If release is granted, the display is blanked to indicate that the self test is ready to start. When the switch is released, self-test commands are issued to the disc drive. One of the first tests is one that causes the **8.8.** display to appear. The display is then blanked until self test is completed. If release is not granted, a **r.d.** (release denied) display will appear. This message will continue to be displayed until the SELF TEST switch is released, at which time the display will show the previous pass/fail result.

When self test has been completed on the units of the disc drive (host dependent controller, disc drive, and power supply), the display will show a **P.x.** (pass) or a **F.x.** (fail) result. The numeral **x.** is the disc drive HP-IB device address.

Note: The decimal points in the display are tied directly to the host dependent controller +5 Vdc supply and signal the presence of this voltage. The decimal points should remain illuminated at all times during both self test and normal operation of the disc drive.

4-14. DISPLAY RESULTS SWITCH

The DISPLAY RESULTS switch is a momentary contact pushbutton switch which causes self test results to be displayed on the Self-Test display. The switch is operated in a similar manner to the SELF TEST switch. When the DISPLAY RESULTS switch is pressed, a request for release is generated. The switch must be pressed and held down until release is granted or denied. If release is granted the display will go blank until the switch is released. If release is denied when the switch is pressed, a **r.d.** message will be displayed. When the switch is released, the previous pass/fail result is restored to the display.

Note: In the event of a self-test failure, the disc drive will have requested release to update the error logs. If the disc drive is not operating correctly, this update operation may take some time to complete. During this period, the DISPLAY RESULTS switch will be inactive. This means that the DISPLAY RESULTS switch may have to be pressed for a longer than normal period of time or pressed after the update operation has been completed.

Following release, pressing the switch a number of times will display a sequence of test failure information. The information displayed for a failure will be, in order, unit failed, field replaceable assembly (FRA) failed, and subtest failed. The failing unit is indicated by the display **U.x.**, where numeral **x.** identifies the unit. The failing FRA is indicated by **A.x.**, where numeral **x.** identifies the FRA. A subtest failed is indicated by a 2-digit hexadecimal number. It is possible for a failing unit to have multiple failing FRA's. Multiple FRA's are listed in descending order of most probable failure. If a unit has no failures to report, it will display only the unit number. Refer to

figure 4-1 for a listing of unit and FRA numbers. Host dependent controller (unit 2) and disc drive (unit 0) subtest numbers, together with a brief description of the subtests, are listed in tables 4-1 and 4-2, respectively.

Note 1. The sequence mode described above is distinct from the pass/fail mode. When sequencing test results, *all* of the results must be displayed before the device will go back on-line (return from release). After the last result has been displayed, the display will return to **P.X.** (pass) or **F.X.** (fail).

Note 2. A unit 2 (host dependent controller) self-test failure is a special type of failure. When unit 2 fails self test, it will enter into an infinite loop monitoring the DISPLAY RESULTS switch. The only function that the disc drive can perform under this condition is to toggle out the unit 2 self-test results. The disc drive will not respond to any commands from the host computer. The red and green FAULT/ON LINE indicators will be illuminated at this time. Exit from the loop can only be achieved by powering down the disc drive.

4-15. INTERNAL DIAGNOSTICS

The disc drive internal diagnostics include self-test routines and run time error and fault reporting circuits. The self-test routines, normally activated at power on, consist of a series of subtests which check overall operation of the disc drive. The disc drive must pass all host dependent controller (unit 2) subtests to come on line. In the event of a device dependent controller (DDC) subtest failure, the disc drive is allowed to come on line. After power on, run time error and fault reporting circuits in disc drive assembly A1 continually monitor certain operations of the disc drive. Run time errors and faults are logged in the disc drive error logs. Details of these two diagnostic tools are provided in the following paragraphs. Refer to table 4-5 for a summary of the diagnostics.

4-16. SELF TEST

The disc drive can execute self-test diagnostic routines which are programmed into the host dependent controller and device dependent controller servo system firmware. When the disc drive is powered on, these routines are automatically initiated to perform a series of subtests which verify operation of the disc drive. The subtests perform many hardware checks first by microdiagnostics and then by higher level macrodiagnostics such as seeks, reads, and writes.

Go/no-go test results are indicated by the FAULT/ON LINE indicator on the front panel of the disc drive and details of subtest failures are presented on the Self Test display on the rear panel. The host can determine details of self-test failures using the CS/80 Request Status command. The internal diagnostics can also be initiated at any time by controls on the rear panel of the disc drive or by the host computer using the Initiate Diagnostic command. Details of the diagnostic tests are provided in the following paragraphs.

4-17. SELF-TEST SUBTESTS

The subtests run during self test can be divided into six functional groups. A general description of the tests in each group, listed in the order that they are performed, is provided in the following paragraphs. Refer to tables 4-1 and 4-2 for a listing of the subtests and the failure conditions detected by the tests.

The first group of subtests (01 through 07, table 4-1) checks the operation of the HDC. The subtests include a short checkout of the HDC microprocessor, a checksum of both the EXEC EPROM and the an exhaustive write/read test of all of the RAM, a loopback test of the DMA gate array IC, a verification of the timer circuitry, and a test of the HP-IB interface IC. A full set of these subtests is run only when self test is initiated at power on. When self test is initiated by either the SELF TEST switch or the host, then only the timer test, the DMA test, and a limited RAM test are performed. This is to protect the existing runtime environment. The subtests described above check the operation of the IC's, circuits, and interfaces resident in the HDC.

The second group of subtests (0AH through 12H, table 4-2) checks the operation of disc drive functions independent of disc drive assembly A1. These subtests include tests of the DDC resident IC's and circuits, a checksum of the device specific PROM, and the sensing of the proper 12 volt power.

The third group of subtests (13H through 1CH, table 4-2) checks the operation of disc drive assembly A1 to the extent of servo activity. The disc drive is selected, a restore command is performed and a few seek commands are issued and monitored for proper completion, direction, and pulse count.

The fourth group of subtests (1DH through 25H, table 4-2) performs further checks of the disc drive assembly A1 servo mechanism, and the read function, as far as position sensing. A scan ID command verifies that the sector headers can be read. A more exhaustive sequence of seeks is then executed, both verifying the subsequent location as well as monitoring the speed performance.

The fifth group of subtests (26H through 5EH, table 4-2) checks seek, read, and write, both one and two sectors, at the inner diameter (ID) and the outer diameter (OD). Reads and writes are also performed on every surface.

The sixth group of tests (5FH through 65H, table 4-2) checks out the error and fault detection circuitry. Circuit tests include: ID not found on a scan ID command, underrun condition, a command aborted, and both ECC correctable and uncorrectable errors.

Note: An additional test is run after a successful initialize and read (subtest 26). This test uses subtests 66H through 68H. The test attempts to read the factory-recorded product number from the disc and match it with the product number resident in the HDA description PROM located in the DDC.

4-18. SELF-TEST ERROR REPORTING

There are three ways which the disc drive reports self-test results to the user. The first way is by means of the front panel FAULT/ON LINE indicator. The second way is via the Self Test display on the rear panel. The third way is by means of the CS/80 Request Status command. The following paragraphs provide details of how these three methods are used to report self-test results.

4-19. FAULT/ON LINE INDICATOR. The red and green LED's which comprise the front panel FAULT/ON LINE indicator signal the operating status of the disc drive. See figure 4-1. A momentary solid red and green display and then a flashing green display occurs when the disc drive is powered on and self test is executing. If the display remains a solid red and green, this means that the host dependent controller (unit 2) has failed self test. At the end of self test, a solid green display indicates that the disc drive has passed self test and is ready for operation. A solid red display indicates that the disc drive has failed self test. When a self-test failure is indicated, the 2-digit hexadecimal Self Test display should be consulted to determine the source of the failure.

4-20. SELF-TEST DISPLAY. The rear panel 2-digit hexadecimal Self Test display (see figure 4-1) will normally show a pass (**P.X.**) or fail (**F.X.**) indication, with **X.** denoting HP-IB address 0 through 7. When the SELF TEST RESULTS switch is used to toggle out results, the display will show all of the results for unit 0, 1, and 2, one unit at a time, until all of the information has been displayed. Unit 0 is the disc drive, unit 1 is not assigned, and unit 2 is the host dependent controller.

Note: The "Unit 2" terminology for the host dependent controller applies only to the disc drive self-test display. The host operating system addresses the controller as unit 15. The "Unit 2" designation for the host dependent controller is used because the self-test display does not have enough digits to present a U15 readout.

Depending on the subtest failed, the display may indicate more than one failed FRA. In the case of multiple FRA failures, the assemblies will be reported in order of most probable failure. Details of the subtest failed follows the FRA failure information. The following is a summary of the 2-digit readout display.

FIRST DIGIT	SECOND DIGIT
U. = Unit number designator	Unit number (0-2) (See figure 4-1)
A. = Field Replaceable Assy number designator	Field Replaceable Assy number (1-6) (See figure 4-1)
P. = Self test pass	HP-IB address (0-7)
F. = Self test fail	HP-IB address (0-7)
0.-6. = Failing self-test subtest number, high digit. (Refer to tables 4-1, 4-2)	0.-F. = Failing self-test subtest number, low digit. (Refer to tables 4-1, 4-2)

The following are examples of typical display readout sequences:

- **SELF TEST PASS**

DISPLAY MESSAGE

P.3. Indicates that unit 0 (disc drive) and unit 2 (host dependent controller) have passed self test. The HP-IB address is set to 3.

- **SELF-TEST FAILURE - UNIT 0 (DISC DRIVE)**

DISPLAY MESSAGE

F.3. Indicates that self test has failed on unit 0 (disc drive) or unit 2 (host dependent controller). The HP-IB address is set to 3. Press and release the DISPLAY RESULTS switch.

U.0. Indicates that unit 0 (disc drive) is ready to report its results upon subsequent operation of the DISPLAY RESULTS switch. (If unit 0 has passed self test and has no results to report, then the next operation of the switch will change the display to **U.2.** to indicate that unit 2 [host dependent controller] will be displaying its results next.) Press and release DISPLAY RESULTS switch.

A.4. Indicates that FRA4 (power supply assembly A4) is the most probable cause of the failure. space 1 **A.2.** Indicates that FRA2 (device dependent controller PCA-A2) is the second most probable cause of the failure. Push and release DISPLAY RESULTS switch.

1.1. Indicates that subtest 11 has failed. This is defined in table 4-2 as "12V threshold bit (bit 0 of DDC self-test register) not set". Press and release DISPLAY RESULTS switch.

U.2. Indicates that unit 2 (host dependent controller), will display its results next. Press and release DISPLAY RESULTS switch.

F.3. Indicates that unit 2 has no results to report and the self-test readout cycle is complete.

- **SELF-TEST FAILURE - UNIT 2 (HOST DEPENDENT CONTROLLER**

DISPLAY MESSAGE

F.3. Indicates that self test has failed on unit 0 (disc drive) or unit 2 (host dependent controller). The HP-IB address is set to 3. Press and release the DISPLAY RESULTS switch.

U.2. Indicates that unit 2 (host dependent controller) has failed self test. Press and release DISPLAY RESULTS switch.

A.5. Indicates that FRA5 (host dependent controller PCA-A5) is the probable cause of the failure. Push and release DISPLAY RESULTS switch.

0.3. Indicates that subtest 03 has failed. This is defined in table 4-1 as "Test of last 15 kilobytes of RAM failed". Press and release DISPLAY RESULTS switch.

F.3. Indicates that self-test readout cycle is complete.

4-21. REQUEST STATUS. If an Initiate Diagnostic command (DIAG) is issued to the disc drive and an execution message returns a QSTAT of 1, this means that a self-test error has occurred. A Request Status command (REQSTAT) should be

issued to get back the reason for the previous QSTAT of 1. When the Request Status command is executed, a 20-byte field is returned. This field is defined in the CS/80 instruction set Programming Manual, part no. 5955-3442. When self test is executed and it fails, the Diagnostic Result Bit (bit 24) will be set in the Fault Error Field (sometimes referred to as the Error Fault Field) of the 20 bytes returned from the Request Status command. When bit 24 is set, P1, P2, P3, P7, and P8 contain specific self-test results, as detailed below:

- P1 - Identifies the most suspect FRA:

  1 = FRA1 (disc drive assembly A1)
  2 = FRA2 (DDC PCA-A2)
  4 = FRA4 (power supply assembly A4)
  5 = FRA5 (HDC PCA-A5)
  6 = Connectors

- P2 - Identifies the next most suspect FRA:

  Same code as P1

- P3 - Failed disc drive (unit 0) self-test subtest. Refer to table 4-2.

- P7 - Failed disc drive error condition. Refer to table 4-3, Disc Drive Error Condition List.

- P8 - Details of failed disc drive error condition. See figure 4-2, P8 Signal Source.

Note: The detailed error condition information given in P8 is obtained from various sources in the disc drive, depending on the test error. In order to identify the reporting source for a particular fault, it is necessary to note the numbers given in P3 (failed self-test subtest) and P7 (disc drive error condition). The point in figure 4-2 where the P3 number (vertical column) and the P7 number (horizontal column) intersect is the reporting source, identified by a letter code. A listing of these codes, together with the information supplied by the identified sources, is provided below.

DE - Data Error Byte

```
LSB 0 = Recoverable
    1 = Marginal
    2 = Marginal (ECC)
    3 = Uncorrectable
MSB 4 = Uncorrectable on write
```

Note: More than one bit may be set. For example, if one location received an uncorrectable error and other locations all had recoverable errors, the data error byte will be set to 09H.

E - Disc Controller IC Error Register

```
LSB 0 = Data address mark not found
    1 = Track 0 error
    2 = Aborted command - Drive not
        ready or write fault
    3 = Unused
    4 = ID not found
    5 = Unused
    6 = CRC error
MSB 7 = Bad block
```

FC - Fault Code List

Refer to table 4-4, Fault Code List.

N - Number of seeks

Specifies the number of seeks performed before failure occurred.

S - Disc Controller IC Status Register

```
LSB 0 = Error bit.
    1 = Command in progress.
    2 = Unused
    3 = DRQ (data request)
    4 = Seek complete
    5 = Write fault
    6 = Drive ready (normally set)
MSB 7 = Busy
```

Z - All zero's. This is a valid subtest number/error condition pairing. However, no additional information is given in P8.

4-22. REQUEST STATUS EXAMPLE. The following example shows how to interpret P1, P2, P3, P7, and P8 returned for a Request Status command following a self-test failure.

P1 = 1
P2 = 2
P3 = 26H
P7 = 3DH
P8 = AEH

P1 and P2 indicate that the most suspect FRA is FRA1 (disc drive assembly A1) and the next most suspect FRA is FRA2 (DDC PCA-A2). P3 indicates that the failed self-test subtest is 26H. This is defined in table 4-2 as "While attempting to read one sector at the outer diameter, either the seek or the read failed". P7 indicates that the disc error condition is 3DH, defined in table 4-3 as "Unit fault". Using P3 and P7 to identify the P8 signal source shows "FC" as the source. This indicates that table 4-4, Fault Code List, should be consulted. Table 4-4 lists AEH as "Verify position operation reveals drive is on the wrong head" as the fault.

4-23. RUN TIME ERROR AND FAULT REPORTING

The return of a QSTAT of 1 following the issuance of a non self-test command to the disc drive implies that a full status should be requested. A Request Status command should thus be issued to get back the reason for the QSTAT of 1. Assuming that a hardware fault or data error of some kind has occurred, the Diagnostic Result Bit (bit 24) will not be set in the Error Fault Field (Fault Error Field) of the 20 bytes returned from the Request Status command. P7 will contain the disc drive fault code and in certain cases, P8 contains additional information.

P7 - Disc fault code. Refer to table 4-4, Fault Code List.

P8 - If P7 is in the range of 50-6F, P8 is disc controller IC error register (**E**). Refer to paragraph 4-21 for details.

If P7 is in the range of 70-8F, P8 is disc controller IC status register (**S**). Refer to paragraph 4-21 for details.

4-24. EXTERNAL EXERCISER

The CS/80 external exerciser is an interpreter which links the disc drive internal diagnostics to a service-trained person. The *CS/80 External Exerciser Reference Manual*, part no. 5955-3462 describes how the exerciser interfaces to CS/80 devices and includes specific information for the HP 7941 and HP 7945 Disc Drives. The following paragraphs briefly describe the functions of the external exerciser commands.

4-25. AMIGO CLEAR (AMCLEAR)

The AMCLEAR command clears the device on the channel which is currently addressed.

4-26. CANCEL TRANSACTION (CANCEL)

The CANCEL command causes graceful termination of most CS/80 transactions, leaving them in the reporting phase.

4-27. TEST HP-IB CHANNEL (CHANNEL)

The CHANNEL command initiates a read and write loopback test over the HP-IB channel.

4-28. CHANNEL INDEPENDENT CLEAR (CICLEAR)

The CICLEAR command will clear any command connected to the channel.

4-29. CLEAR LOGS (CLEAR LOGS)

The CLEAR LOGS command clears the run-time data error log, the error rate test log, and the fault log.

4-30. DESCRIBE SELECTED UNIT (DESCRIBE)

The DESCRIBE command allows information within the currently addressed unit to be sent to the HP 85.

4-31. PERFORM INTERNAL DIAGNOSTICS (DIAG)

The DIAG command invokes diagnostic routines which reside in the internal device controller firmware. The DIAG command has three parameter bytes. The first two of these bytes are

an integer loop count. The third byte is a diagnostic test number. This command may be directed to unit 15 (HDC) or unit 0 (disc drive).

If the command is directed to unit 15, the valid value range for the diagnostic test number parameter is 0 through 3. These values correspond to the following tests:

0 = Full Run Time Self Test. Performs the following three HDC tests as well as the unit 0 self test.

1 = HDC RAM Test. Performs the two pass RAM test on an empty 1k data buffer. RAM allocated to the units and/or the operating system is not tested.

2 = DMA Test. Performs the DMA test run at power-on.

3 = Timer Test. Performs the timer test run at power-on.

If the command is directed to unit 0, the valid value range is also 0 through 3. These values correspond to the following tests:

0 = Unit 0 DDC power-on self test. This does not include the HDC self test; however, the entire power-on DDC self test is performed.

1 = Random Seek Test. A total of 256 seeks are performed per loop.

2 = Full Stroke Seek Test. A total of 256 seeks from outer diameter (OD) to inner diameter (ID) are performed per loop.

3 = Incremental Seek. Performs successive one-track seeks from OD to ID and back again.

4-32. OUTPUT ERROR RATE TEST LOG (ERT LOG)

The ERT LOG command allows access to the error rate test log which contains an accumulation of all read errors which were found during a read-only or write-then-read error rate test. Error rate test errors are accumulated until the log is cleared using the CLEAR LOGS command.

4-33. EXIT PROGRAM (EXIT)

The EXIT command causes the CS/80 external exerciser program to exit.

4-34. OUTPUT FAULT LOG (FAULT LOG)

The FAULT LOG command allows access to the fault log, an accumulation of the faults which have occurred on the disc drive since the last time a CLEAR LOGS command was issued.

4-35. OUTPUT HELP INFORMATION (HELP)

The HELP command prints all of the command names.

4-36. INITIALIZE MEDIA (INIT MEDIA)

The INIT MEDIA utility performs an initialization routine on the disc drive. The INIT MEDIA utility has a valid value of B, P, and I. These values correspond to the following:

B = Initializes the logic region. Spare table, spare tracks, sector headers, and logs are left intact.

P = Initializes the logic region and field spares are deallocated. Factory spares and logs are unchanged.

I = Initializes the entire drive. Logical tracks, spare tracks, and maintenance tracks are cleared. The spare table (factory and field spares) is written back onto the maintenance tracks.

4-37. UPDATE DEVICE LOGS (PRESET)

The PRESET command causes all recent information in controller RAM to be logged on the disc maintenance tracks.

4-38. REQUEST STATUS (REQSTAT)

The REQSTAT utility sends a status message from the device to the exerciser.

4-39. PERFORM READ-ONLY ERROR RATE TEST (RO ERT)

The RO ERT command allows a sequential or random read to take place in order to locate any read errors.

4-40. OUTPUT RUN LOG (RUN LOG)

The RUN LOG command allows access to the run log which contains an accumulation of all read errors which were found during run time. Run-time data errors are accumulated until the log is cleared using the CLEAR LOGS command.

4-41. SPARE (SPARE)

The SPARE utility physically relocates a track to an address which is reserved for sparing.

4-42. OUTPUT SPARE TABLE (SPARE TABLE)

The SPARE TABLE command accesses the information in the spare table.

4-43. OUTPUT DEVICE TABLE (TABLES)

The TABLES command accesses the tables stored internally within the device in order to determine the operational status of the device.

4-44. PERFORM SERVO TEST (SERVO)

The SERVO test checks the operation of the servo system. An exhaustive sequence of seeks is executed verifying the subsequent location as well as monitoring the speed performance. The entire sequence of seeks is repeated six times.

4-45. SET UNIT NUMBER (UNIT)

The UNIT utility allows the user to select the unit number to be addressed within the device. The disc drive is unit 0.

4-46. PERFORM WRITE-THEN-READ ERROR RATE TEST (WTR ERT)

The WTR ERT command writes a predefined data pattern over a specified area of the disc, then reads all data which was written.

4-47. TROUBLESHOOTING

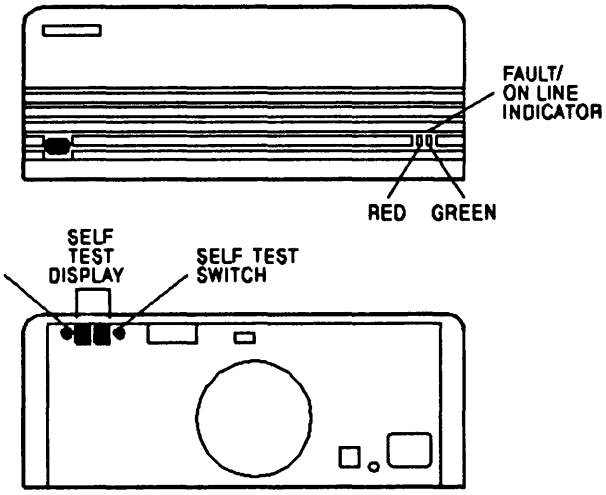
When troubleshooting the disc drive, the first thing to do is to determine if the fault is repeatable or intermittent. A repeatable fault usually causes the same self-test fail result to be presented each time self test is performed. An intermittent fault, on the other hand, occurs at random intervals, and may not always cause a self-test failure.

In the case of a repeatable fault, self test will identify the failing FRA with a 95 percent certainty. In the event that more that one FRA is listed as the possible cause of the failure, replace the FRA's, one at a time, in the order given in the self-test display.

Note: Cable faults (an open cable conductor, loose cable connector, etc.) may present a multiple FRA failure message. The FRA's listed will be the FRA's at either end of the defective cable. All cabling should therefore be checked before replacing any FRA's.

Note: Cables W1 and W3 are sufficiently long to allow FRA1 (disc drive assembly A1) to be connected into circuit adjacent to the disc drive cabinet. This allows a substitute FRA1 to be connected into circuit without removing FRA1 from the cabinet.

Attempt to isolate the fault to a specific FRA by running self test following the replacement of each FRA.



FAULT/ON LINE INDICATOR

RED	GREEN	
ON	ON	INDICATOR TEST FOR 1 SECOND AFTER INITIATING SELF TEST OR CONTROLLER (U2) FAILED SELF TEST.
OFF	FLASHING	EXECUTING SELF TEST OR DISC DRIVE ACTIVE.
OFF	ON	DISC DRIVE PASSED SELF TEST OR DISC DRIVE INACTIVE.
ON	OFF	DISC DRIVE FAILED SELF TEST;READY FOR DIAGNOSTICS
ON	FLASHING	DISC DRIVE FAILED SELF TEST;TEST ROUTINES STILL ACTIVE

SELF TEST DISPLAY

DISPLAY	MESSAGE	
8.8.	DISPLAY TEST	GO/NO-GO TEST RESULT
P.*	SELF TEST PASS. *=HP-IB ADDRESS	
F.*	SELF TEST FAIL. *=HP-IB ADDRESS	
rd	RELEASE DENIED	
U.0.	UNIT 0 (DISC DRIVE)	UNIT FAILED
U.2.	UNIT 2 (HOST DEPENDENT CONTROLLER)	
A.1.	DISC DRIVE FRA1	FIELD REPLACEABLE ASSEMBLY (FRA) FAILED
A.2.	DDC FRA2	
A.4.	POWER SUPPLY FRA4	
A.5.	HDC FRA5	
A.6.	CONNECTORS	
0.0.	UNIT 0/	
⋮	UNIT 2 SELF-TEST	
⋮	SUBTEST FAILED	
⋮	SEE	
6.1.	TABLES 4-1 AND 4-2	
8.8.	FOR LISTINGS	

FILE=FSJEF22B

Figure 4-1. Self-Test Controls and Readout

Table 4-1. Host Dependent Controller (Unit 2) Self-Test Subtest List

READOUT (HEX)	SUBTEST
	GROUP 1
88	Microprocessor failed.
01	Test of the first 1 kilobyte of RAM failed.
02	Checksum of EXEC EPROM failed.
03	Test of last 15 kilobyte of RAM failed.
04	DMA machine test failed.
05	HDC timer circuitry not within specification.
06	HP-IB interface test failed.
07	Configuration failure - cannot find a valid unit 0.

Table 4-2. Disc Drive (Unit 0) Self-Test Subtest List

READOUT (HEX)	SUBTEST
	GROUP 2
0A	PUPO register written and was 0FH when read back.
0B	Value read from PUPO register was not value written.
0C	DMA loopback test failed transfer into DMA RAM.
0D	DMA loopback test failed transfer out of DMA RAM.
0E	Write to 2^3 head select line did not set head bit 3 (bit 1 of DDC self-test register).
0F	Write to 2^3 head select line did not clear head bit 3 (bit 1 of DDC self-test register).
10	Device specific PROM read into RAM - subsequent checksum failed.
11	12 volt threshold bit (bit 0 of DDC self-test register) not set.
12	Value read from a disc controller IC register not value written.
	GROUP 3
13	Timeout occurred after drive selected while waiting for drive ready status.
14	Restore Command issued and failed.
15	Seek completed, seek complete bit is not set in the disc controller IC status, but is set in bit 3 of DDC self-test register.
16	Seek command completed, Seek complete not set in either disc controller IC status or the self-test register.
17	Seek command failed, disc controller IC status register indicates reason.
18	Seek command failed, disc controller IC error register indicates reason.
19	Seek completed, but pulse count was not 1, as expected.
1A	Seek completed, but pulse count was not 15 as expected.
1B	Seek completed, but the direction bit (bit 2 of the DDC self-test register) did not indicate it.
1C	Seek completed, but the direction bit did not indicate out.

Table 4-2. Disc Drive (Unit 0) Self-Test Subtest List (Continued)

READOUT (HEX)	SUBTEST
	GROUP 4
1D	Scan ID failed due to data error.
1E	Scan ID failed, reason indicated in disc controller IC status register.
1F	Scan ID failed, reason indicated in disc controller IC error register.
20	A seek failed in the seek test, command did not complete.
21	A seek failed in the seek test, command completed - but no seek complete status.
22	A seek failed in the seek test, command completed in failure.
23	A Scan ID failed in the seek test.
24	A Scan ID in the seek test indicates that the drive is on the wrong track.
25	Was not able to complete all the seeks in the seek test within the allotted time.
	GROUP 5
26	While attempting to read one sector at the outer diameter, either the seek or the read failed.
27	While attempting a write then read of one sector at the OD, either the seek or the write failed.
28	While attempting a write then read of one sector at the OD, either the read failed, or the data read did not match that written.
29	While attempting a write then read of one sector on surface 0, either the seek of the write failed.
2A	While attempting a write and then read of one sector on surface 0, either the read failed, or the data read did not match that written.
2B	After a successful write then read of one sector on every surface (with a unique pattern for each surface), test produced a seek failure, a read failure, or data different from that written.
2C	While attempting a write then read of one sector on surface 1, either the seek of the write failed.
2D	While attempting a write and then read of one sector on surface 1, either the read failed, or the data read did not match that written.

Table 4-2. Disc Drive (Unit 0) Self-Test Subtest List (Continued)

READOUT (HEX)	SUBTEST
2E	After a successful write then read of one sector on every surface (with a unique pattern for each surface), test produced a seek failure, a read failure, or data different from that written.
2F	While attempting a write then read of one sector on surface 2, either the seek of the write failed.
30	While attempting a write and then read of one sector on surface 2, either the read failed, or the data read did not match that written.
31	After a successful write then read of one sector on every surface (with a unique pattern for each surface), test produced a seek failure, a read failure, or data different from that written.
32	While attempting a write then read of one sector on surface 3, either the seek of the write failed.
33	While attempting a write and then read of one sector on surface 3, either the read failed, or the data read did not match that written.
34	After a successful write then read of one sector on every surface (with a unique pattern for each surface), test produced a seek failure, a read failure, or data different from that written.
35	While attempting a write then read of one sector on surface 4, either the seek of the write failed.
36	While attempting a write and then read of one sector on surface 4, either the read failed, or the data read did not match that written.
37	After a successful write then read of one sector on every surface (with a unique pattern for each surface), test produced a seek failure, a read failure, or data different from that written.
38	While attempting a write then read of one sector on surface 5, either the seek of the write failed.
39	While attempting a write and then read of one sector on surface 5, either the read failed, or the data read did not match that written.
3A	After a successful write then read of one sector on every surface (with a unique pattern for each surface), test produced a seek failure, a read failure, or data different from that written.
3B	While attempting a write then read of one sector on surface 6, either the seek of the write failed.
3C	While attempting a write and then read of one sector on surface 6, either the read failed, or the data read did not match that written.

Table 4-2. Disc Drive (Unit 0) Self-Test Subtest List (Continued)

READOUT (HEX)	SUBTEST
3D	After a successful write then read of one sector on every surface (with a unique pattern for each surface), test produced a seek failure, a read failure, or data different from that written.
3E thru 55	Reserved for future use.
56	While attempting to read two sectors at the OD, either the seek or the read failed.
57	While attempting a write then read of two sectors at the OD, either the seek or the write failed.
58	While attempting a write then read of two sectors at the OD, either the read failed, or the data read did not match that written.
59	While attempting to read one sector at the inner diameter (ID), either the seek or the read failed.
5A	While attempting a write then read of one sector at the ID, either the seek or the write failed.
5B	While attempting a write then read of one sector at the ID, either the read failed, or the data read did not match that written.
5C	While attempting to read two sectors at the ID, either the seek or the read failed.
5D	While attempting a write then read of two sectors at the ID, either the seek or the write failed.
5E	While attempting a write then read of two sectors at the ID, either the read failed, or the data read did not match that written.
	GROUP 6
5F	A read command was issued for a non-existent sector. The expected ID not found error was not detected.
60	A read was performed with the DMA disabled. The expected overrun in condition was not detected.
61	The drive was deselected and a seek command issued. The expected command aborted status was not detected.
62	ECC correctable test, write full operation failed.
63	ECC correctable test, read operation failed or the data was miscorrected.
64	ECC uncorrectable test, write full operation failed.

Table 4-2. Disc Drive (Unit 0) Self-Test Subtest List (Continued)

READOUT (HEX)	SUBTEST
65	ECC uncorrectable test, read operation failed or value read indicated that correction was attempted.
66	Product number, cannot be read.
67	Product number, value read was unitialized.
68	Product number, wrong number.

Table 4-3. Disc Drive Error Condition List

READOUT (HEX)	ERROR CONDITION
30	Miscompare.
31	Failed.
32	Passed second scan ID on different head.
33	Data errors occurred on every location.
34	Seek timeout - disc controller IC has not completed command.
35	Seek timeout - Command completed - seek complete bit not set.
36	Seek - write fault.
37	Seek - drive not ready.
38	Seek fault.
39	R/W data byte count invalid.
3A	Command aborted.
3B	Disc controller IC timeout - reset.
3C	Disc controller IC timeout - cannot reset.
3D	Unit fault.
3E	Fault occurred, but unable to identify condition.
3F	Verify position failure.

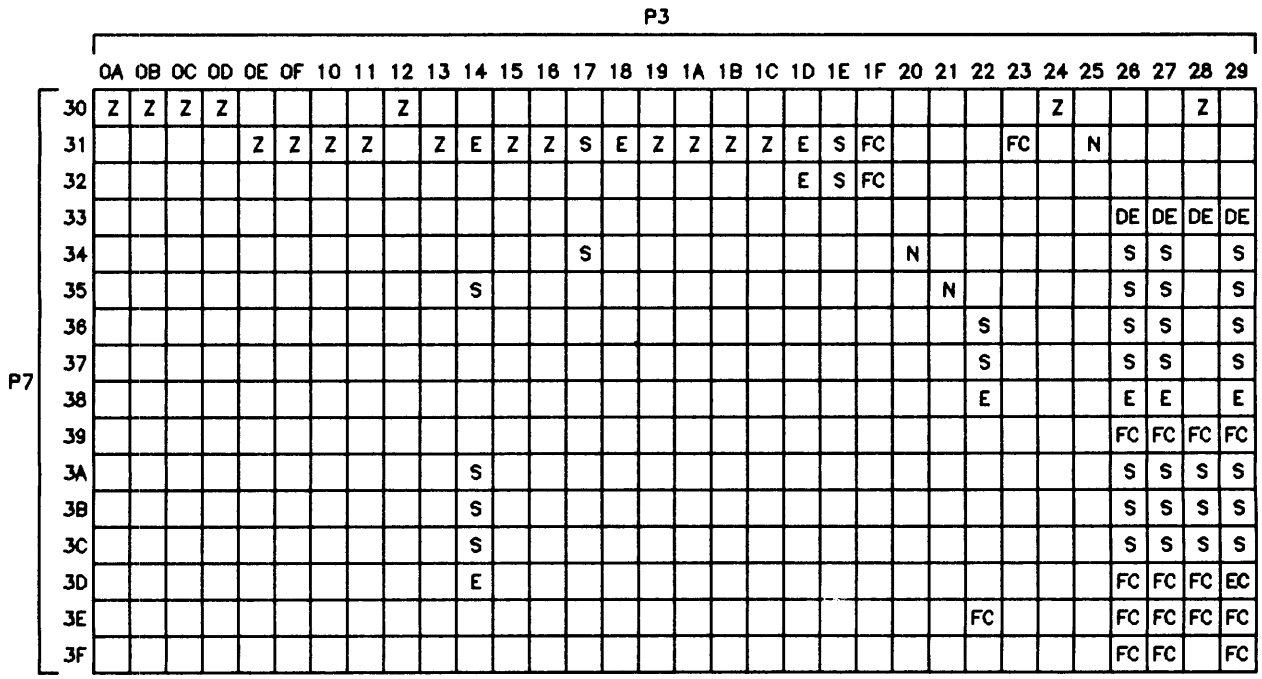
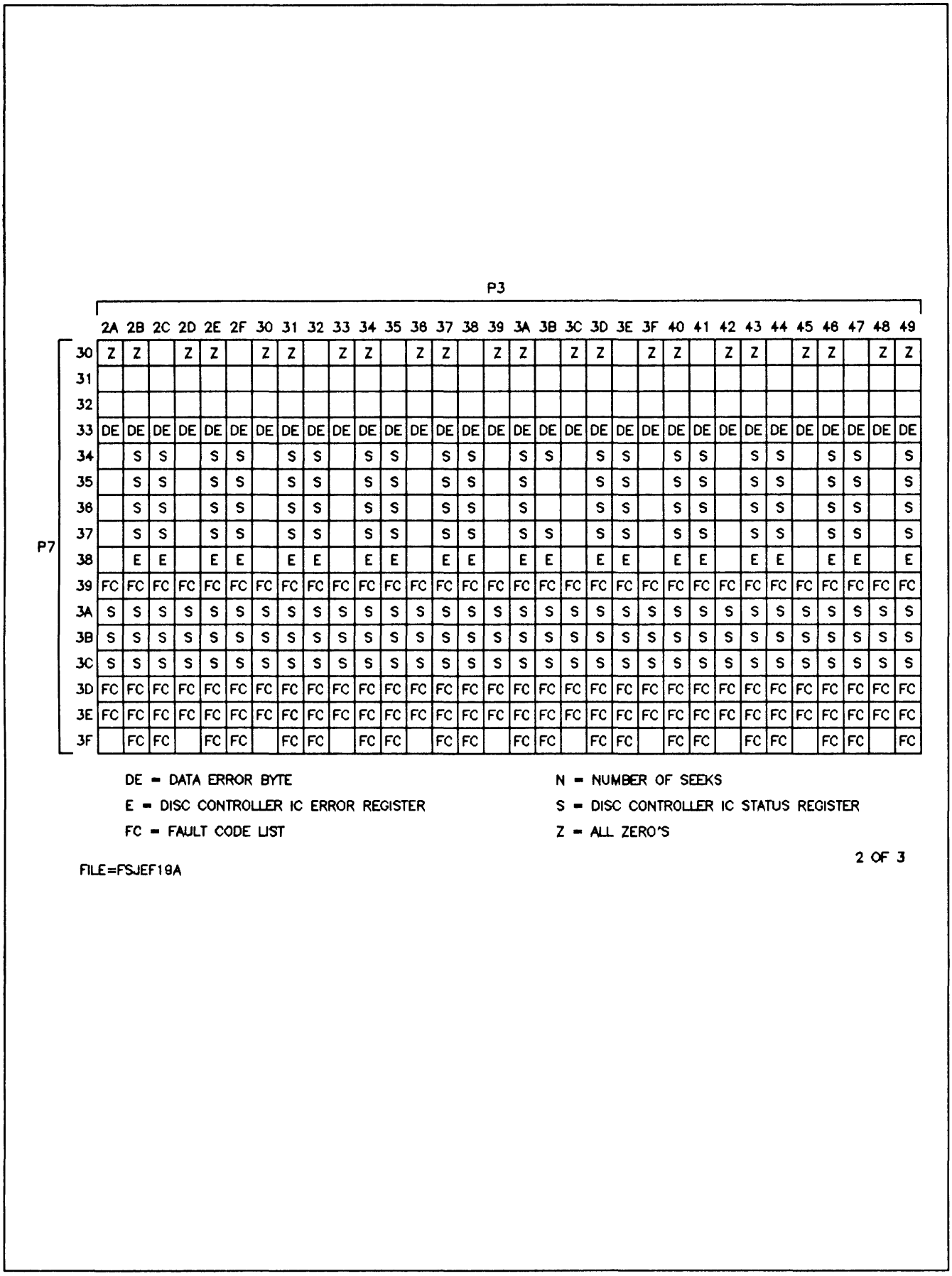


Figure 4-2. P8 Signal Source (Sheet 1 of 3)



P3

P7	2A	2B	2C	2D	2E	2F	30	31	32	33	34	35	36	37	38	39	3A	3B	3C	3D	3E	3F	40	41	42	43	44	45	46	47	48	49
30	Z	Z		Z	Z		Z	Z		Z	Z		Z	Z		Z	Z		Z	Z		Z	Z		Z	Z		Z	Z		Z	Z
31																																
32																																
33	DE	DE	DE	DE	DE	DE	DE	DE	DE	DE	DE	DE	DE	DE	DE	DE	DE	DE	DE	DE	DE	DE	DE	DE	DE	DE	DE	DE	DE	DE	DE	DE
34		S	S		S	S		S	S		S	S		S	S		S	S		S	S		S	S		S	S		S	S		S
35		S	S		S	S		S	S		S	S		S	S		S			S	S		S	S		S	S		S	S		S
36		S	S		S	S		S	S		S	S		S	S		S			S	S		S	S		S	S		S	S		S
37		S	S		S	S		S	S		S	S		S	S		S	S		S	S		S	S		S	S		S	S		S
38		E	E		E	E		E	E		E	E		E	E		E	E		E	E		E	E		E	E		E	E		E
39	FC	FC	FC	FC	FC	FC	FC	FC	FC	FC	FC	FC	FC	FC	FC	FC	FC	FC	FC	FC	FC	FC	FC	FC	FC	FC	FC	FC	FC	FC	FC	FC
3A	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S
3B	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S
3C	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S
3D	FC	FC	FC	FC	FC	FC	FC	FC	FC	FC	FC	FC	FC	FC	FC	FC	FC	FC	FC	FC	FC	FC	FC	FC	FC	FC	FC	FC	FC	FC	FC	FC
3E	FC	FC	FC	FC	FC	FC	FC	FC	FC	FC	FC	FC	FC	FC	FC	FC	FC	FC	FC	FC	FC	FC	FC	FC	FC	FC	FC	FC	FC	FC	FC	FC
3F		FC	FC		FC	FC		FC	FC		FC	FC		FC	FC		FC	FC		FC	FC		FC	FC		FC	FC		FC	FC		FC

DE = DATA ERROR BYTE
E = DISC CONTROLLER IC ERROR REGISTER
FC = FAULT CODE LIST
N = NUMBER OF SEEKS
S = DISC CONTROLLER IC STATUS REGISTER
Z = ALL ZERO'S

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Figure 4-2. P8 Signal Source (Sheet 2 of 3)

P3

P7	4A	4B	4C	4D	4E	4F	50	51	52	53	54	55	56	57	58	59	5A	5B	5C	5D	5E	5F	60	61	62	63	64	65	66	67	68
30		Z	Z		Z	Z		Z	Z		Z	Z			Z			Z			Z					Z		Z			Z
31																						Z	Z	Z		FC		FC		Z	
32																															
33	DE	DE	DE	DE	DE	DE	DE	DE	DE	DE	DE	DE	DE	DE	DE	DE	DE	DE	DE	DE	DE		E		DE	DE	DE	DE			
34	S		S	S		S	S		S	S		S	S	S		S	S		S	S			S		S						
35	S		S	S		S	S		S	S		S	S	S		S	S		S	S			S		S						
36	S		S	S		S	S		S	S		S	S	S		S	S		S	S			S		S						
37	S		S	S		S	S		S	S		S	S	S		S	S		S	S			S		S						
38	E		E	E		E	E		E	E		E	E	E		E	E		E	E			E		E						
39	FC	FC	FC	FC	FC	FC	FC	FC	FC	FC	FC	FC	FC	FC	FC	FC	FC	FC	FC	FC	FC				FC	FC	FC	FC			
3A	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S		S		S	S	S	S			
3B	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S		S		S	S	S	S			
3C	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S		S		S	S	S	S			
3D	FC	FC	FC	FC	FC	FC	FC	FC	FC	FC	FC	FC	FC	FC	FC	FC	FC	FC	FC	FC	FC				FC	FC	FC	FC	Z		
3E	FC	FC	FC	FC	FC	FC	FC	FC	FC	FC	FC	FC	FC	FC	FC	FC	FC	FC	FC	FC	FC		FC		FC	FC	FC	FC			
3F	FC		FC	FC		FC	FC		FC	FC		FC	FC	FC		FC	FC		FC	FC			FC		FC						

DE = DATA ERROR BYTE
E = DISC CONTROLLER IC ERROR REGISTER
FC = FAULT CODE LIST
N = NUMBER OF SEEKS
S = DISC CONTROLLER IC STATUS REGISTER
Z = ALL ZERO'S

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Figure 4-2. P8 Signal Source (Sheet 3 of 3)

Table 4-4. Fault Code List

Oct	Dec	Hex	Miscellaneous Errors Caused by Externally Initiated Operations
00	00	00	No error.
01	01	01	End of volume.
02	02	02	Power on.
03	03	03	Address bounds error.
04	04	04	Low on spare tracks.
05	05	05	Spare table overflow.
06	06	06	Parameter bounds error on a utility.
07	07	07	Maintenance track overflow - logs are full. (or sector count has overflowed).
			Data Errors
40	32	20	Recoverable data error.
41	33	21	Marginal data error - more than one try recovered the data.
42	34	22	Marginal data error - correction operation was used to recover the data.
43	35	23	Uncorrectable data error.
44	36	24	Recoverable data error - ID field.
45	37	25	Marginal - ID field.
47	39	27	Unrecoverable - ID field.
50	40	28	Recoverable - data address mark not found.
51	41	29	Marginal - data address mark not found.
53	43	2B	Unrecoverable - data address mark not found.
57	47	2F	Unrecoverable data error on write operation (ID field not readable).
			General faults that don't map to a specific status error bit. Self Test Errors
60	48	30	Miscompare.
61	49	31	Failed.
62	50	32	Passed second scan ID on different head.
63	51	33	Data error occurred on every location.
64	52	34	Seek timeout - disc controller IC has not completed command.
65	53	35	Seek/Restore timeout - no seek complete.
66	54	36	Seek - write fault.
67	55	37	Seek - drive not ready.
70	56	38	Seek fault.
71	57	39	R/W DMA byte count invalid.
72	58	3A	Write fault - drive not ready.
73	59	3B	Disc controller IC timeout - reset.
74	60	3C	Disc controller IC timeout - cannot reset.
75	61	3D	Unit fault.
76	62	3E	Fault occurred, but unable to identify condition.
77	63	3F	Verify position failure.

Table 4-4. Fault Code List (Continued)

Oct	Dec	Hex	Controller Faults
100	64	40	
101	65	41	Memo sequence error.
102	66	42	No empty memos available.
103	67	43	Too many commands queued.
115	77	4D	Bad execution vector from decoder.
116	78	4E	Byte - underrun bit of DDC errors register set.
117	79	4F	DMA-In. Wrong byte count (DMA never completed). DMA-Out. Wrong byte count (DMA never completed).
			Unit Faults with Disc Controller IC Error Register (Refer to "E - Disc Controller IC Error Register", paragraph 4-21, on how to interpret the P8 error byte.)
121	81	51	Unit fault during read or write.
123	83	53	Unit fault during scan ID.
124	84	54	Unit fault during verify operation.
125	85	55	Unit fault during correction operation.
126	86	56	Retries exhausted on full sector operation.
134	92	5C	Track 000 error on restore.
135	93	5D	Unit fault on restore.
136	94	5E	Format - unit fault.
137	96	5F	Unit fault during seek operation.
			Unit faults with Disc Controller IC Status Register (Refer to "S - Disc Controller IC Status Register", paragraph 4-21, on how to interpret the P8 status byte.)
160	112	70	Write fault on retry of Seek
161	113	71	Drive not readyon retry of Seek
162	114	72	Seek retry fault
163	115	73	Scan ID failed before retry of Seek
164	116	74	Seek timeout fault - 3 seconds
165	117	75	Seek retried
166	118	76	Seek retry timed out - 300 msec
200	128	80	Format - write fault.
201	129	81	Unit fault during read or write.
202	130	82	Aborted command on read or write.
203	131	83	Disc controller IC timeout on read or write. IC has been reset.
204	132	84	Disc controller IC timeout on read or write. IC will not reset.
205	133	85	Disc controller IC timeout during verify.
206	134	86	Disc controller IC timeout during scan ID command.
207	135	87	Disc controller IC timeout during seek.
210	136	88	Disc controller IC timeout during correction.
211	137	89	Drive not ready or write fault on restore.
212	138	8A	Restore completed but no seek complete.
213	139	8B	Restore - disc controller IC timeout - disc controller IC reset.
214	140	8C	Drive not ready on seek.
215	141	8D	Write fault on seek.
216	142	8E	Restore - disc controller IC timeout - disc controller IC will not reset.

Table 4-4. Fault Code List (Continued)

Oct	Dec	Hex	Unit Faults
220	144	90	Read spare table timeout.
221	145	91	Format - Sector count register not zero.
222	146	92	Format - DMA transfer count not valid.
223	147	93	Format - timeout.
224	148	94	Infinite loop detected in logical address mapping - Spare tables lost.
225	149	95	Spare tables read failure
226	150	96	Store spare tables failure.
227	151	97	Read serial number failure.
230	152	98	Write serial number failure.
236	158	9E	Track sparing failed - lost spare tables.
237	159	9F	Zeroing of spare tracks operation failed in Deallocate Spares.
240	160	A0	Seek to deallocated spare failed in Deallocate Spares.
241	161	A1	Copy of track to be spared has failed.
242	162	A2	Write of spare track failed, spare allocated but not assigned.
243	163	A3	Track Sparing cannot obtain resources.
244	164	A4	Track Sparing failed while writing spare tables to disc.
245	165	A5	Verify failed on second spare track.
246	166	A6	Seek failure during verify of spare tracks.
247	167	A7	Disc controller IC error bit set but no error found.
250	168	A8	Write fault during operation other than write (Write current present in head.)
252	170	AA	Disc controller IC overran the DMA (IC register must have glitched).
253	171	AB	Seek Complete will not come true after a write fault.
255	173	AD	ID-not found on scan ID command. Restore performed.
256	174	AE	Verify position operation reveals drive is on the wrong head.
257	175	AF	Verify position operation reveals drive is on the wrong cylinder.
266	182	B6	Write retries on this sector exhausted - due to write fault.
300	192	C0	Unit fault - logs unreadable.

Table 4-5. Diagnostic Summary

UNIT 0 AND UNIT 2 SELF TEST

SELF TEST

1. 78 Subtests. Subtests indicated on rear panel 2-digit hexadecimal display
   Subtest code range: 0A-68H (unit 0), 00-07, 88 (unit 2).

2. 16 supplementary error condition codes. Error code range; 30-3F.

SELF TEST REPORTING, UNIT 0 and UNIT 2

1. Front panel FAULT/ON LINE indicator: pass/fail.

2. Rear panel 2-digit hexadecimal readout:
   - Failed unit.
   - Failed FRA(s).
   - Failed subtest.

SELF TEST REPORTING, UNIT 0

1. QSTAT=1

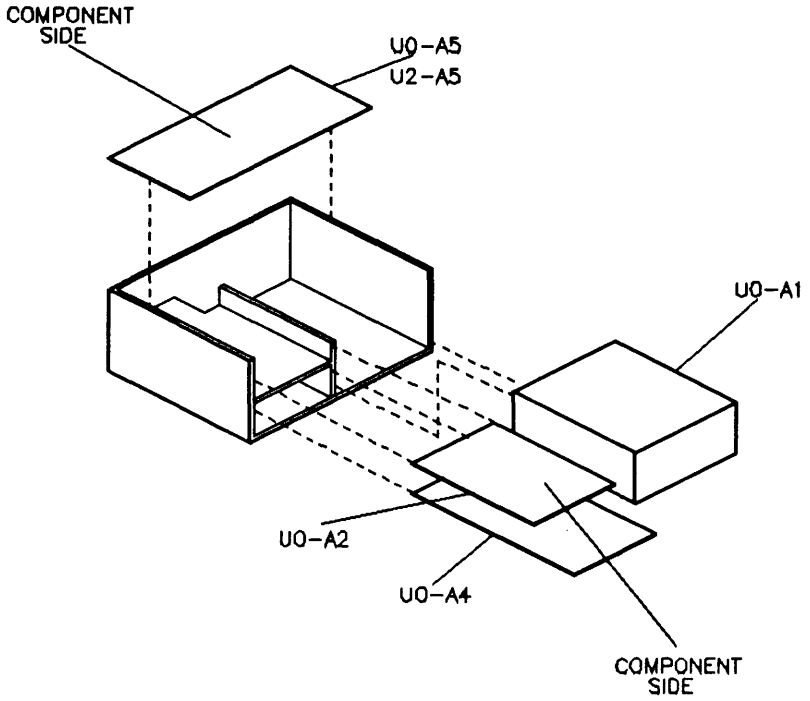
2. REQUEST STATUS message format:
   - Bit 24 set
   - P1: Most likely failed FRA
   - P2: Second most likely failed FRA
   - P3: Failed subtest
   - P7: Failed error condition
   - P8: Supplementary error codes - data error byte, disc controller IC error register, fault code list, number of seeks, and disc controller IC status register.

UNIT 0 RUN TIME ERROR AND FAULT REPORTING

RUN TIME ERROR AND FAULT REPORTING

1. QSTAT=1.

2. REQUEST STATUS message format:
   - Bit 24 not set.
   - P7: Fault code list
   - P8: Supplementary error codes - disc controller IC error and status registers.
3. Log entries
   - All faults/data error codes logged in fault log/data error log.
   - Data error address, status byte occurrence count logged in run log.



U (UNIT)	A (FIELD REPLACEABLE ASSEMBLY)
0-DISC DRIVE	1-DISC DRIVE A1 2-DEVICE DEPENDENT CONTROLLER PCA-A2 4-POWER SUPPLY A4 5-HOST DEPENDENT CONTROLLER PCA-A5 6-CONNECTORS (NOT SHOWN)
2-CONTROLLER	5-HOST DEPENDENT CONTROLLER PCA-A5

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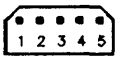
Figure 4-3. Field Replaceable Assembly (FRA) Locations

1. J1 PINS ARE NUMBERED 1 THRU 20. EVEN-NUMBERED PINS ARE ON SOLDER SIDE OF PCA. THERE IS A KEYSEAT BETWEEN PINS 4 AND 6.

2. J2 PINS ARE NUMBERED 1 THRU 34. EVEN-NUMBERED PINS ARE ON SOLDER SIDE OF PCA. THERE IS A KEYSEAT BETWEEN PINS 4 AND 6.

3. J3 IS NUMBERED AS SHOWN



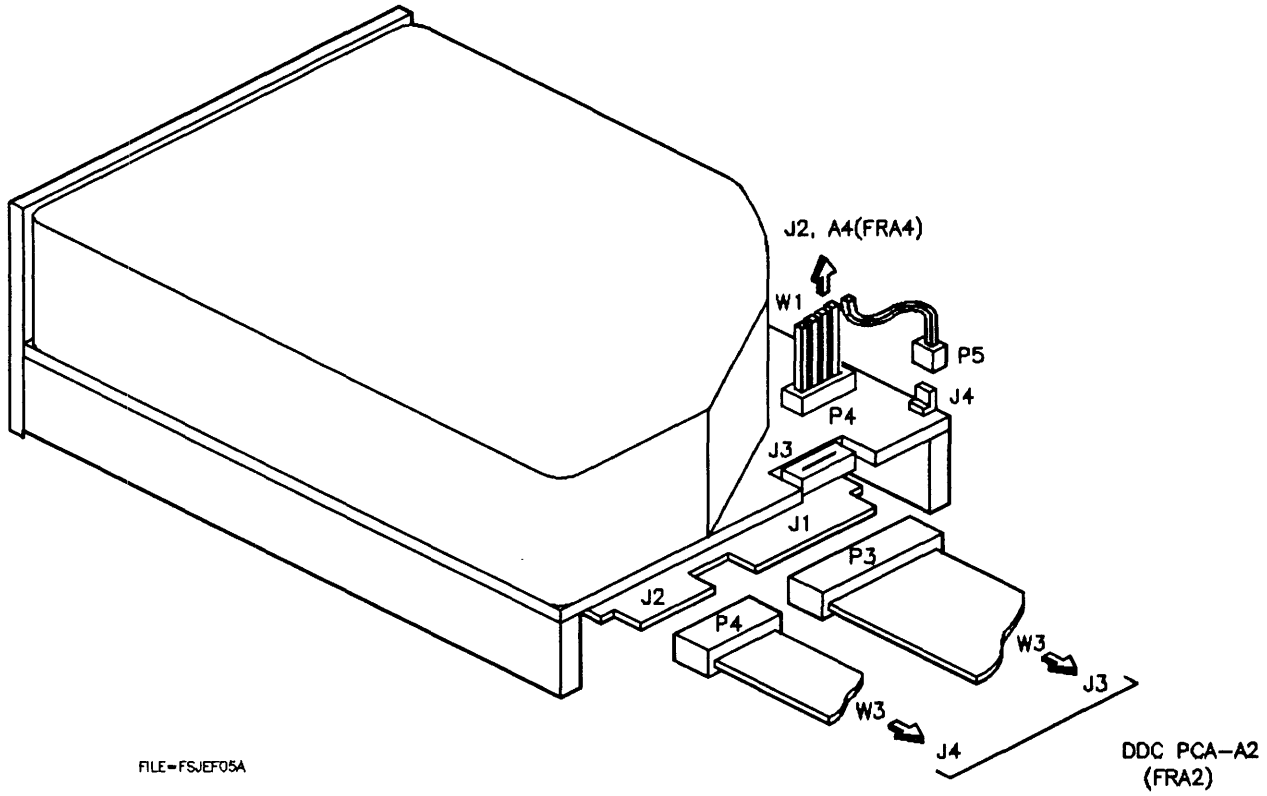


Figure 4-4. FRA1 (Disc Drive A1), Layout and Cable Connections

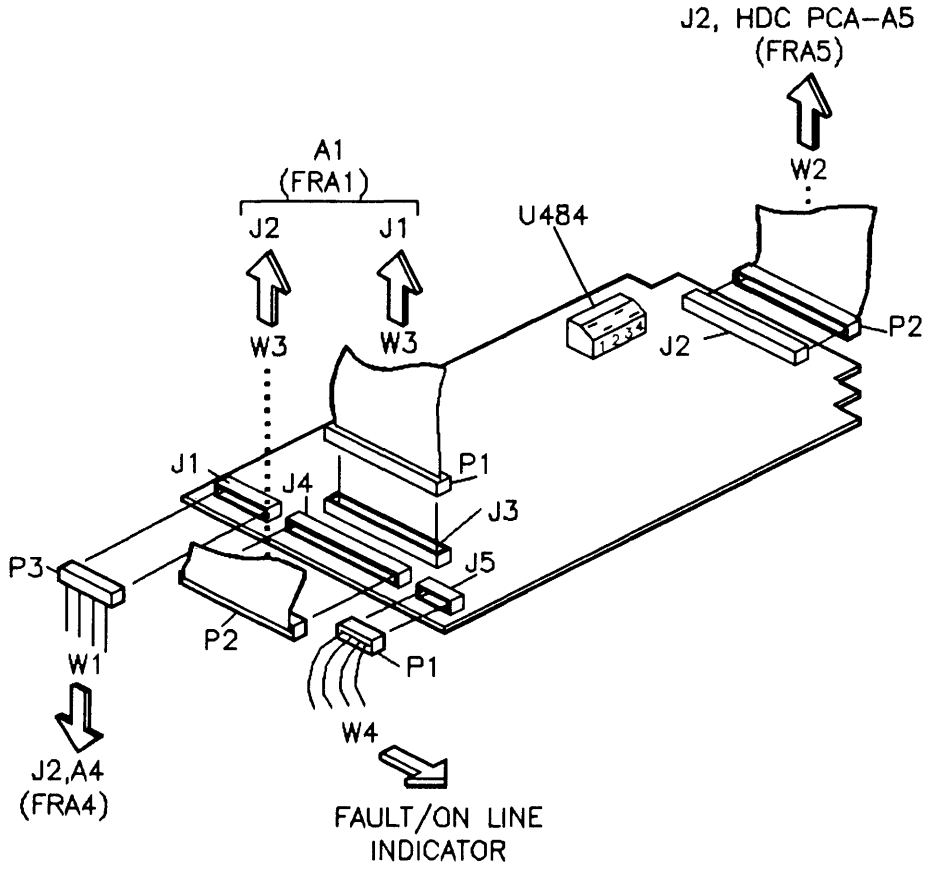


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Figure 4-5. FRA2 (DDC PCA-A2), Layout and Cable Connections

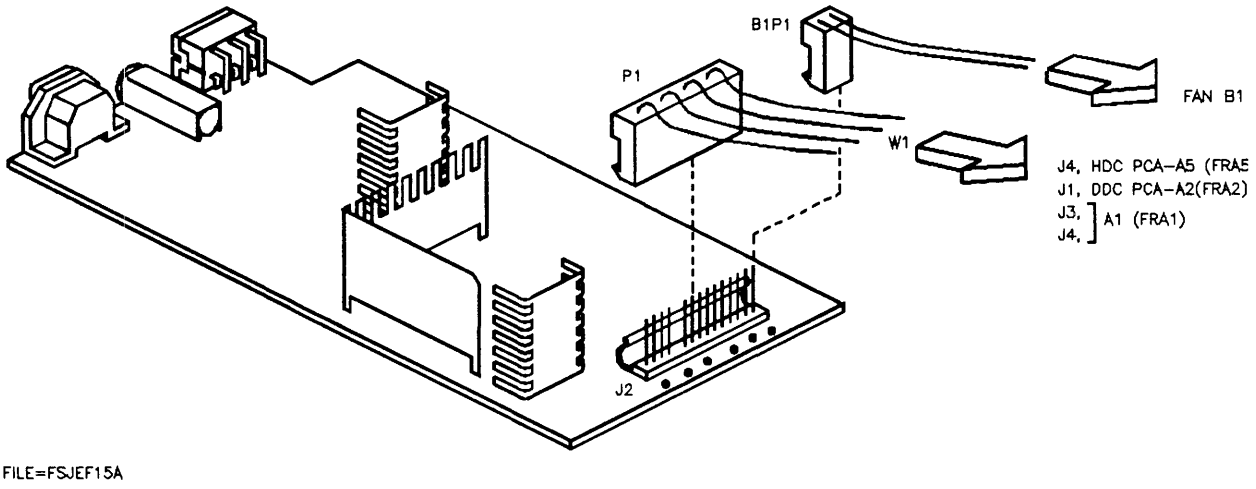


Figure 4-6. FRA4 (Power Supply A4), Layout and Cable Connections

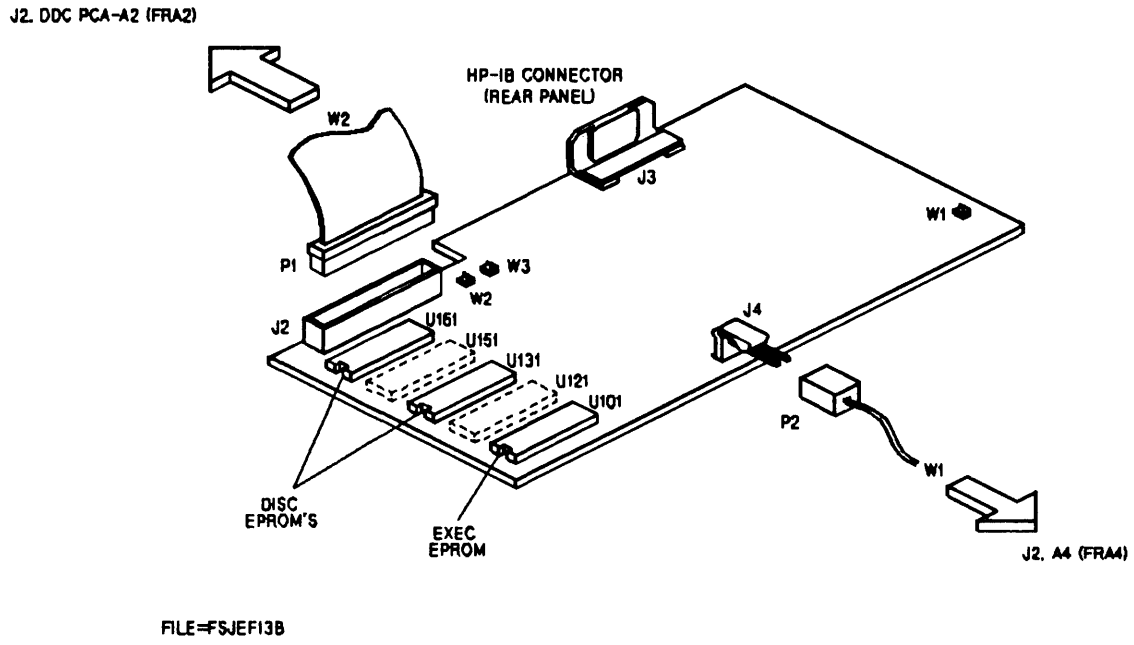
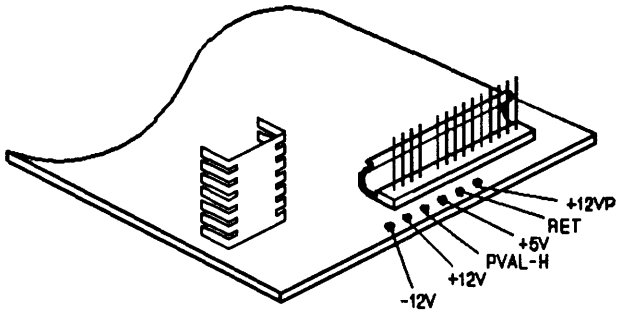


Figure 4-7. FRA 5 (HDC PCA-A 5), Layout and Cable Connections



TEST POINT	VOLTAGE RANGE
-12V	-11.4 TO -12.6V
+12V	+11.64 TO +12.36V
PVAL-H	≥ +2.4V (TYPICALLY 4.0V)
+5V	+4.85 TO 5.15V
+12VP	11.0 TO 13.0V

NOTE:
1. -12V IS NOT USED IN THE HP7941 AND HP7945.
2. USE RET TEST POINT FOR VOLTMETER RETURN.
3. THE OUTPUT VOLTAGES ARE NOT ADJUSTABLE.
4. MAXIMUM RIPPLE:
   5V SUPPLY: <50mV P-P
   12V SUPPLIES: <100mV P-P

Figure 4-8. FRA4 (Power Supply A4), Test Points and Voltages

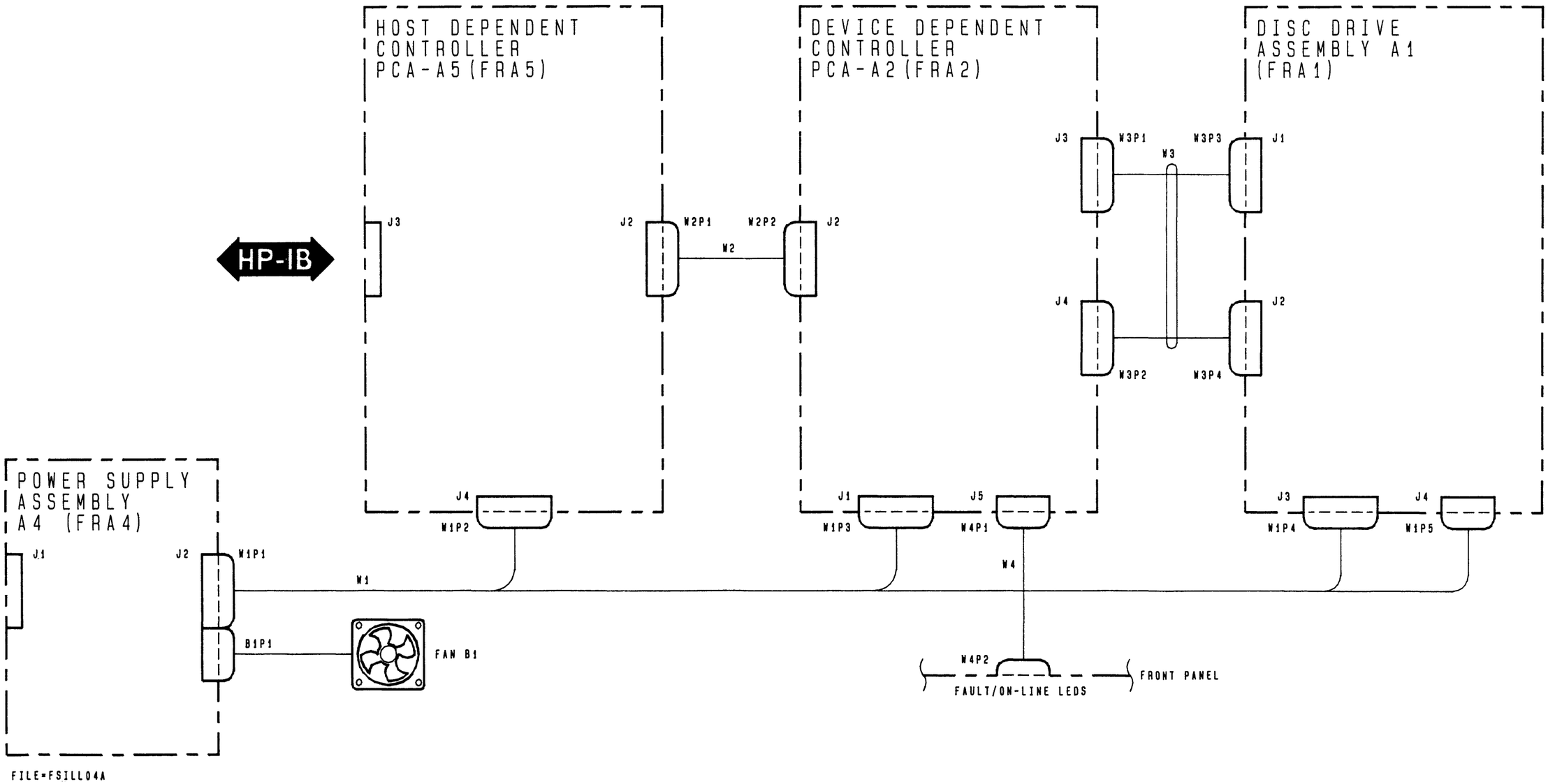
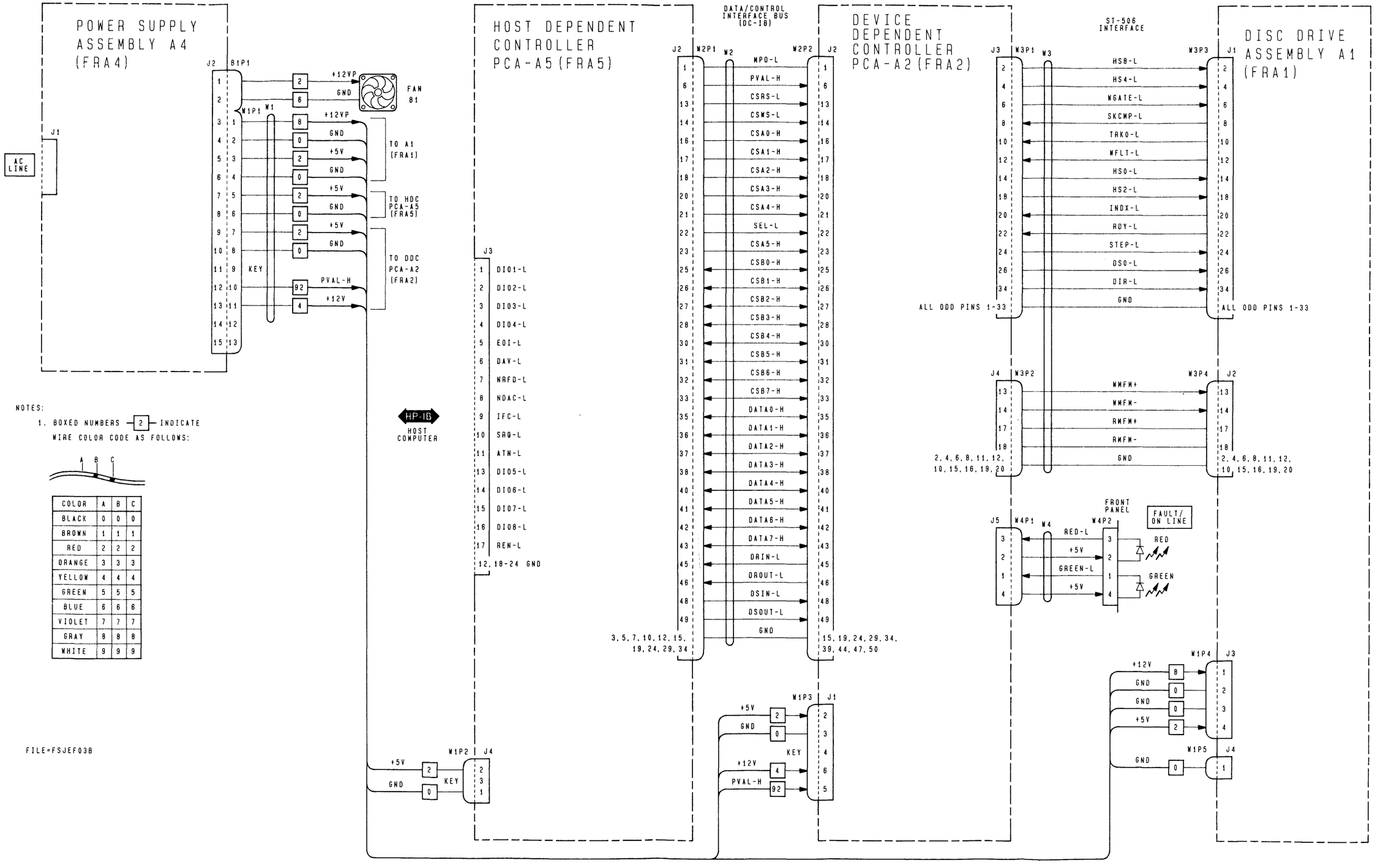


Figure 4-9. Cabling Diagram



NOTES:

1. BOXED NUMBERS — 2 — INDICATE WIRE COLOR CODE AS FOLLOWS:

COLOR	A	B	C
BLACK	0	0	0
BROWN	1	1	1
RED	2	2	2
ORANGE	3	3	3
YELLOW	4	4	4
GREEN	5	5	5
BLUE	6	6	6
VIOLET	7	7	7
GRAY	8	8	8
WHITE	9	9	9

FILE=FSJEF03B

Figure 4-10. Signal Distribution

REMOVAL AND REPLACEMENT

SECTION V

5-1. INTRODUCTION

WARNING

The disc drive does not contain operator serviceable parts. To prevent electrical shock, refer all service activities to service-trained personnel.

CAUTION

- The field replaceable assemblies (FRA's) in the disc drive are electrostatic-sensitive devices. Take appropriate precautions when removing the FRA's from the disc drive. Use of an anti-static pad and wrist strap is required. (These components are contained in anti-static work station, part no. 9300-0749.) Immediately after removal, store the FRA's in anti-static, conductive plastic bags.

- The disc drive is delicate and should be handled with care. Also, the disc drive is heavier (9.9 kilograms/21.8 pounds) than its size would indicate.

- Do not turn the LINE~ switch on or off when the system is transferring data on the Hewlett-Packard Interface Bus (HP-IB).

- Do not cycle the LINE~ switch on and off unnecessarily.

- Do not connect or disconnect the HP-IB cable assembly(s) from the disc drive when the system is transferring data on the HP-IB.

This section provides removal and replacement procedures for field replaceable assemblies (FRA's) and parts in the disc drive. Procedures are given in the order in which disassembly normally occurs. Each part or assembly which must be removed before access can be gained to another assembly or part is presented first, followed by the next assembly which can be removed. This disassembly order is shown in figure 5-1. The locations of the FRA's are shown in figure 4-3. Figures 4-4 through 4-7 identify the connectors on the FRA's and their mating cable assembly connectors. Figure 4-9 provides an overall cabling diagram of the disc drive. References are also made to figure 6-1, Disc Drive, Exploded View, to assist in identifying and locating parts.

Note: TORX* hardware is used in the disc drive. This hardware requires the use of special drivers. In this manual, any reference to this type of hardware will be accompanied by the required driver size (for example, "T15").

5-2. PREPARATION FOR SERVICE

Before starting any removal or replacement procedure, prepare the disc drive for service as follows:

a. Set the disc drive LINE~ switch to the 0 (out) position and disconnect the power cord from the ~AC LINE connector.

b. Disconnect the HP-IB cable assembly from the disc drive HP-IB connector.

c. Place the disc drive on the anti-static pad and connect the wrist strap to the pad. When the top

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shroud is removed, (paragraph 5-4), ground the frame of the disc drive to the pad.

CAUTION

Ensure that the anti-static wrist strap is attached to the wrist before removing or replacing any components in the disc drive.

5-3. REMOVAL AND REPLACEMENT

Removal and replacement instructions for field replaceable assemblies (FRA's) and parts in the disc drive are provided in the following paragraphs. Unless otherwise specified, replacement is a reversal of the removal instructions.

5-4. TOP SHROUD

To remove the top shroud (1, figure 6-1), proceed as follows:

a. Perform the preparation for service procedure outlined in paragraph 5-2.

b. Ensure that the power cord is disconnected from the ~AC LINE connector on the rear panel of the disc drive.

c. Remove the three T10 screws (2, figure 6-1) which secure the top shroud to the disc drive.

d. Raise the rear of the top shroud upwards slightly and then move it backwards and away from the disc drive.

e. Ground the frame of the disc drive to the anti-static pad.

Reinstallation is a reversal of the removal procedure.

5-5. EPROM KITS

To remove the EXEC EPROM kit (3, figure 6-1) and/or the DISC EPROM kit (4), proceed as follows:

a. Perform the preparation for service procedure outlined in outlined in paragraph 5-2. Pay particular attention to the instructions given for use of the anti-static pad and wrist strap.

b. Ensure that the power cord is disconnected from the ~AC LINE connector on the rear panel of the disc drive.

c. Remove the top shroud (refer to paragraph 5-4).

d. Remove the single EXEC EPROM (3) from the 28-pin socket U101 on FRA5 (5). See figure 4-7 for the location of U101. Place the EPROM on a piece of anti-static foam.

e. Remove the two DISC EPROM's (4) from 28-pin sockets U131 and U161 on FRA5 (5). See figure 4-7. Place the EPROM's on a piece of anti-static foam.

Reinstallation is a reversal of the removal procedure. The EXEC EPROM is labeled U101 and the DISC EPROM's are labeled U131 and U161. Ensure that the EPROMS are installed in their matching 28-pin sockets on FRA5 (5), with the index notches on the EPROM's facing toward the edge of FRA5. See figure 4-7.

5-6. FRA5 (HOST DEPENDENT CONTROLLER PCA-A5)

To remove FRA5 (5, figure 6-1) from the disc drive, proceed as follows:

a. Perform the preparation for service procedure outlined in paragraph 5-2.

b. Ensure that the power cord is disconnected from the ~AC LINE connector on the rear panel of the disc drive.

c. Remove the top shroud (refer to paragraph 5-4).

d. Remove the two 6-32 hex standoffs (6) and lock washers (7) which secure the HP-IB connector on FRA5 (5) to the rear panel of the disc drive.

e. Disconnect connector P2 on power cable assembly W1 (23) from connector J4 on FRA5 (5)

f. Disconnect connector P1 on ribbon cable assembly W2 (22) from connector J2 on FRA5 (5)

g. Slide FRA5 (5) forward and out of the disc drive.

Reinstallation is a reversal of the removal procedure. Before installing FRA5, ensure that there is a circuit board jumper (5A) in place on the two "DISK OR TAPE" pins at W2 on FRA5. Ensure also that there is a circuit board jumper (5A) in place on the two pins at W1. See figure 4-7 for the locations of W1 and W2. Install the EPROM kits (3, 4) as described in paragraph 5-5. Ensure also that the cable assembly connectors disconnected in steps e and f are firmly seated in their mating connectors.

5-7. FRONT PANEL

To remove the front panel (15, figure 6-1) from the disc drive, proceed as follows:

a. Perform the preparation for service procedure outlined in paragraph 5-2.

b. Ensure that the power cord is disconnected from the ~AC LINE connector on the rear panel of the disc drive.

c. Remove the top shroud (refer to paragraph 5-4).

d. Remove the four T10 screws (8) which secure the front shield (14), with front panel (15) and LED cable assembly W4 (10) attached, to the disc drive. Move the front panel forward away from the disc drive.

e. Disconnect connector P1 on LED cable assembly W4 (10) from connector J5 on FRA2 (21) and remove the front panel (15) from the disc drive.

f. If it is necessary to remove the front panel shield (14) from the front panel (15), proceed as follows:

(1) Remove the clip (9) which secures cable assembly W4 (10) to the front panel shield (14).

(2) Remove the four T25 screws (13) which secure the front panel shield (14) to the front panel (15).

(3) Remove the front panel shield (14) from the front panel (15).

Reinstallation is a reversal of the removal procedure. Ensure that the cable assembly connector disconnected in step e is properly seated in its mating connector. Check also that the LINE~ switch operates freely before tightening the four T10 screws (8) removed in step d.

5-8. FAN

To remove the fan (16, figure 6-1) from the disc drive, proceed as follows:

a. Perform the preparation for service procedure outlined in paragraph 5-2.

b. Ensure that the power cord is disconnected from the ~AC LINE connector on the rear panel of the disc drive.

c. Remove the top shroud (refer to paragraph 5-4), FRA5 (refer to paragraph 5-6), and the front panel (refer to paragraph 5-7).

d. Remove the four T20 screws (17) and grille (18), which secure the fan (16) to the rear panel.

Note: In early production runs of the disc drive, the fan attaching parts consist of four T15 machine screws, four captive nuts, and grille. (See figure 6-1 in Appendix A.)

e. Disconnect the fan (16) power cable connector B1P1 from connector J2 on FRA4 (27).

f. Disengage the fan cable assembly from the two cable clamps (37) and remove the fan from the disc drive.

Reinstallation is a reversal of the removal procedure. Ensure that the fan is positioned with its power cable assembly in line with the cable clamps (37). Ensure also that the cable assembly connector disconnected in step e is firmly seated in its mating connector. Before returning the disc drive to service, check that the fan is operating correctly.

5-9. FRA2 (DDC PCA-A2)

To remove FRA2 (21) from the disc drive, proceed as follows:

a. Perform the preparation for service procedure outlined in paragraph 5-2.

b. Ensure that the power cord is disconnected from the ~AC LINE connector on the rear panel of the disc drive.

c. Remove the top shroud (refer to paragraph 5-4) and the front panel (refer to paragraph 5-7).

d. Disconnect connector P3 on power cable assembly W1 (23) from connector J1 on FRA2 (21).

e. Disconnect connectors P1 and P2 on ribbon cable assembly W3 (20) from connectors J3 and J4, respectively, on FRA2 (21).

f. Disconnect connector P1 on LED cable assembly W4 (10) from connector J5 on FRA2 (21).

g. Disconnect connector P1 on ribbon cable assembly W2 (22) from connector J2 on PCA-A5 (5).

h. Carefully slide FRA2 (21), with cable assembly W2 (22) attached, out of the disc drive.

i. Disconnect connector P2 on ribbon cable assembly W2 (22) from connector J2 on FRA2 (21) and remove the cable assembly.

Reinstallation is a reversal of the removal procedure. Before installing FRA2 in the disc drive, ensure that switch U484 in FRA2 is set as follows. Refer to figure 4-5 for the location of U484.

```
HP 7945: 1 - open (up)
         2 - closed (down)
         3 - open (up)
         4 - closed (down)

HP 7941: 1 - open (up)
         2 - closed (down)
         3 - closed (down)
         4 - closed (down)
```

Ensure also that the cable assembly connectors disconnected in steps d through g and step i are properly seated in their mating connectors.

5-10. FRA4 (POWER SUPPLY ASSEMBLY A4)

To remove FRA4 (27) from the disc drive, proceed as follows:

a. Perform the preparation for service procedure outlined in paragraph 5-2.

b. Ensure that the power cord is disconnected from the ~AC LINE connector on the rear panel of the disc drive.

c. Remove the top shroud (refer to paragraph 5-4) and the front panel (refer to paragraph 5-7).

d. Disconnect connector P1 on power cable assembly W1 (23) from connector J2 on FRA4 (27).

e. Disconnect the fan (16) cable assembly connector B1P1 from connector J2 on FRA4 (27).

f. Remove the T10 screw (24) and spacer (25) which secure FRA4 (27) to the mainframe assembly (38).

g. Remove the two T15 screws (26) which secure FRA4 (27) to the mainframe assembly (38).

h. Slide FRA4 (27) forward and out of the disc drive.

Reinstallation is a reversal of the removal procedure. Check that the cable assembly connectors disconnected in steps d and e are properly seated in their mating connector. Ensure that the T10 screw (24), and spacer (25) removed in step f are properly installed. Ensure also that the two T15 screws (26) removed in step g are properly replaced. This attaching hardware is required to properly ground the power supply to the mainframe assembly of the disc drive.

5-11. FRA1 (DISC DRIVE ASSEMBLY A1)

To remove FRA1 (34, figure 6-1) from the disc drive, proceed as follows.

Note: Before removing FRA1, refer to paragraph 4-47. This describes how to use a substitute FRA1 to verify the operation of FRA1 without removing it from the disc drive.

a. Perform the preparation for service procedure outlined in paragraph 5-2.

b. Ensure that the power cord is disconnected from the ~AC LINE connector on the rear panel of the disc drive.

c. Remove the top shroud (refer to paragraph 5-4) and the front panel (refer to paragraph 5-7).

d. Disconnect connectors P3 and P4 on ribbon cable assembly W3 (20) from connectors J1 and J2, respectively, on FRA1 (34).

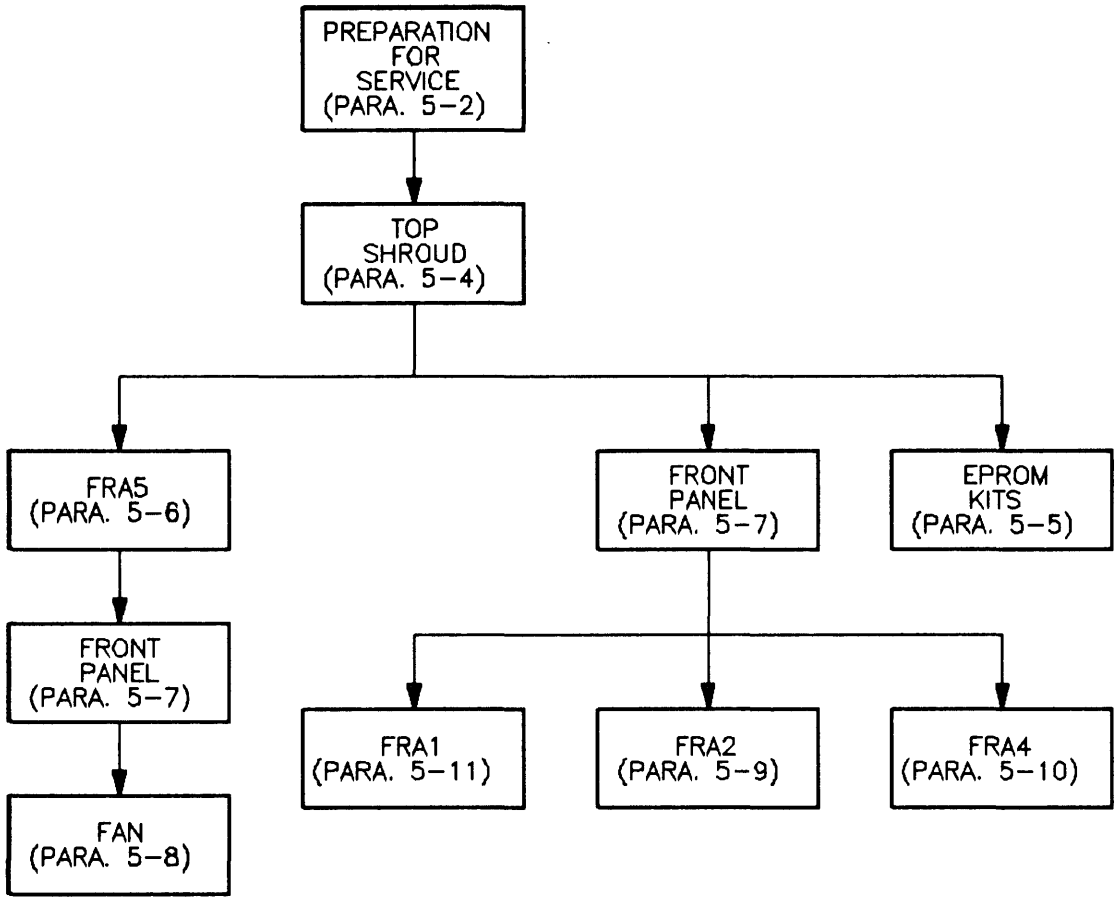
e. Disconnect connectors P4 and P5 on power cable assembly W1 (23) from connectors J3 and J4, respectively, on FRA1 (34).

f. Remove the three T15 screws (35) which secure FRA1 (34) to the mainframe assembly (38).

g. Remove the T10 screw (36) which secures FRA1 (34) to the mainframe assembly (38).

h. Carefully withdraw FRA1 (34) from the mainframe assembly (38).

Reinstallation is a reversal of the removal process. Ensure that the cable assembly connectors disconnected in steps d and e are firmly seated in their mating connectors.



FRA1 – DISC DRIVE A1

FRA2 – DEVICE DEPENDENT CONTROLLER PCA-A2

FRA4 – POWER SUPPLY A4

FRA5 – HOST DEPENDENT CONTROLLER PCA-A5

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Figure 5-1. Order of Disassembly

REPLACEABLE PARTS

SECTION VI

6-1. INTRODUCTION

This section provides listings of all field-replaceable parts and an illustrated parts breakdown for the disc drive. Replaceable parts ordering information for the disc drive is also provided in this section.

Replaceable parts for the disc drive are listed in order of disassembly in table 6-1 and illustrated in figure 6-1. In each listing, attaching parts are listed immediately after the item they attach. Items in the DESCRIPTION column are indented to indicate their relationship to the next higher assembly. In addition, the symbol "---x---" follows the last attaching part for the item. Identification of the items and the labels is as follows:

Major Assembly

*Replaceable Assembly

*Attaching Part for Replacement Assembly

**Subassembly or Component Part

**Attaching Part for Subassembly or Replacement Part

The replaceable parts listings provide the following information for each part:

a. FIG & INDEX NO. The figure and index number which indicates where the replaceable part is illustrated.

b. HP PART NO. The Hewlett-Packard number for the replaceable part.

c. DESCRIPTION. The description of the replaceable part.

Refer to table 6-2 for an explanation of the abbreviations used in the DESCRIPTION column.

d. MFR CODE. The 5-digit code that denotes a typical manufacturer of a part. Refer to table 6-3 for a listing of manufacturers that correspond to the codes.

e. MFR PART NO. The manufacturer's part number for each replaceable part.

f. UNITS PER ASSEMBLY. The total quantity of each part used in the major assembly.

g. The MFR CODE and MFR PART NO. for common hardware are listed as 00000 and OBD (order by description), respectively, because these items can usually be purchased locally.

Note: TORX* hardware is used in the disc drive. This hardware requires the use of special drivers. In this manual, any reference to this type of hardware will be accompanied by the required driver size (for example, "T15").

6-2. ORDERING INFORMATION

To order replaceable parts for the disc drive, address the order to your local Hewlett-Packard Sales and Support Office. Sales and Support Offices are listed at the back of this manual. Specify the following information for each order:

a. Model and full serial number.

b. Hewlett-Packard part number.

c. Complete description of each part as provided in the replaceable parts listing.

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Table 6-1. Disc Drive Replaceable Parts

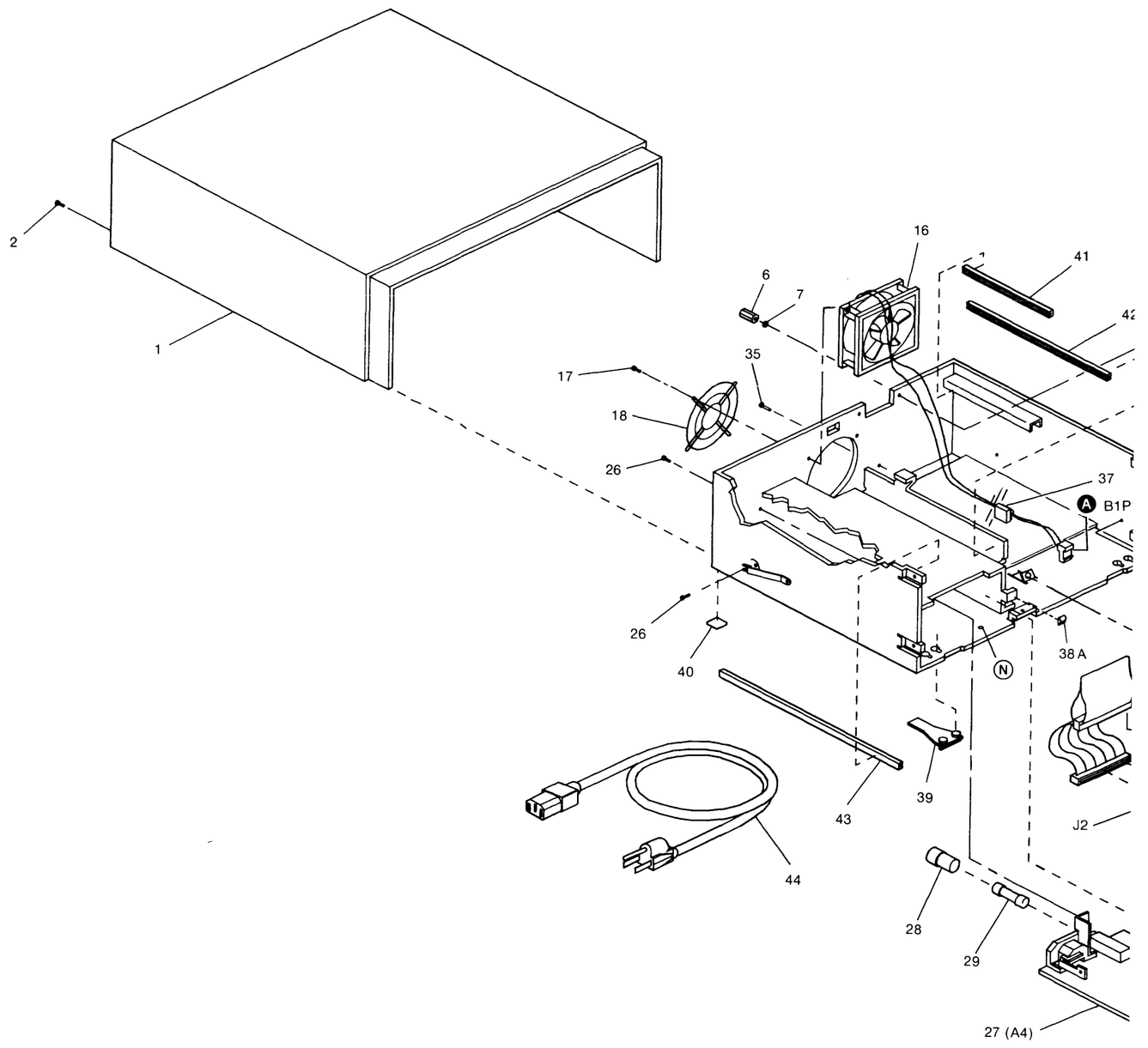
FIG.& INDEX NO.	HP PART NO.	DESCRIPTION	MFR CODE	MFR PART NO.	UNITS PER ASSY
6-1-	7941A	DISC DRIVE	28480	7941A	REF
	7945A	DISC DRIVE	28480	7945A	REF
1	07940-60028	*TOP SHROUD ASSEMBLY (Attaching Parts)	28480	07940-60028	1
2	0515-0372	*SCREW, machine, pnh, T10, M3.0 by 0.5, 8 mm long, w/scw - - - X - - -	00000	OBD	3
3	07940-10105	*EPROM KIT, EXEC	28480	07940-10105	1
4	07940-10203	*EPROM KIT, DISC	28480	07940-10203	1
5	07940-60195	*HOST DEPENDENT CONTROLLER PCA (A5/FRA5)	28480	07940-60195	1
5A	1285-0221	**JUMPER, circuit board (W1, W2/W3) (Attaching Parts)	28480	1285-0221	2
6	0380-0643	*STANDOFF, hex, 6-32, 0.255 in. long	28480	0380-0643	2
7	2190-0017	*WASHER, lock, helical, no. 8 - - - X - - -	00000	OBD	2
8	0515-0372	*SCREW, machine, pnh, T10, M3.0 by 0.5, 8 mm long, w/scw	00000	OBD	4
9	07940-00068	*CLIP	28480	07940-00068	1
10	07941-60033	*CABLE ASSEMBLY (W4)	28480	07941-60033	1
11	1990-0929	**LED, red	28480	1990-0929	1
12	1990-0930	**LED, green	28480	1990-0930	1
13	0624-0590	*SCREW, tapping, pnh, T25, 8-16, 0.312 in. long	00000	OBD	4
14	07940-60026	*SHIELD, front panel	28480	07940-60026	1
15	07941-60010	*FRONT PANEL ASSEMBLY, 7941	28480	07941-60010	1
	07945-60010	*FRONT PANEL ASSEMBLY, 7945	28480	07945-60010	REF
16	07941-60019	*FAN (Attaching Parts)	28480	07941-60019	1
17	0624-0661	**SCREW, tapping, pnh, T20, 10-14, 0.625 in. long	00000	OBD	4
18	07941-00026	*GRILLE, fan	28480	07941-00026	1
19		Not assigned - - - X - - -			
20	07941-60008	*CABLE ASSEMBLY (W3)	28480	07941-60008	1
21	07941-60102	*DEVICE DEPENDENT CONTROLLER PCA (A2/FRA2)	28480	07941-60102	1
22	07941-60007	*CABLE ASSEMBLY (W2)	28480	07941-60007	1
23	07941-60009	*CABLE ASSEMBLY (W1)	28480	07941-60009	1
24	0515-0665	*SCREW, machine, pnh, T10, M3.0 by 0.5, 14 mm long, w/scw	00000	OBD	1
25	0380-1746	*SPACER	28480	0380-1746	1
26	0515-0433	*SCREW, machine, pnh, T15, M4.0 by 0.70, 8 mm long, w/scw	00000	OBD	2
27	07940-60094	*POWER SUPPLY ASSEMBLY (A4/FRA4)	28480	07940-60094	1
28	2110-0565	**FUSEHOLDER, cap	28480	2110-0565	1
29	2110-0003	**FUSE, 3A, 250V, nontime delay 0.250 in. Dia., 1.250 in. long	75915	2A250V3.0A	1
30	5041-1203	**CAP	28480	5041-1203	1
31	0380-1655	**HOLDER, shaft	28480	0380-1655	1

Table 6-1. Disc Drive Replaceable Parts, (Continued)

FIG.& INDEX NO.	HP PART NO.	DESCRIPTION	MFR CODE	MFR PART NO.	UNITS PER ASSY
32	09133-40202	**SHAFT, switch	28480	09133-40202	1
33	09144-45404	**SHIELD, power supply	28480	09144-45404	1
34	07941-60021	*DISC DRIVE ASSEMBLY, 7941 (A1/FRA1)	28480	07941-60021	1
	07945-60021	*DISC DRIVE ASSEMBLY, 7945 (A1/FRA1)	28480	07945-60021	REF
		(Attaching Parts)			
35	0515-0433	*SCREW, machine, pnh, T15, M4.0 by 0.70, 8 mm long, w/scw	00000	OBD	3
36	0515-0372	*SCREW, machine, pnh, T10, M3.0 by 0.50, 8 mm long, w/scw	00000	OBD	1
		- - - X - - -			
37	1400-0510	*CLAMP, cable	02768	8511-28-00-9901	2
38	07941-60074	*MAINFRAME ASSEMBLY	28480	07941-60074	1
38A	8160-0280	**CONTACT, finger	28480	8160-0280	1
39	09121-48303	**FOOT, front	28480	09121-48303	2
40	0403-0427	**FOOT, rear	94959	SJ-5008	2
41	0403-0268	**GUIDE, PCA, 5 in. long	28480	0403-0268	2
42	0403-0302	**GUIDE, PCA, 8 in. long	28480	0403-0302	2
43	0403-0379	**GUIDE, PCA, 9.9 in. long	28480	0403-0379	2
44	8120-1378	*POWER CORD ASSEMBLY, NEMA5A/CEE	28480	8120-1378	1
	8120-1351	*POWER CORD ASSEMBLY, BS 1363/CEE	28480	8120-1351	REF
	8120-1369	*POWER CORD ASSEMBLY, ASC 112/CEE	28480	8120-1369	REF
	8120-1689	*POWER CORD ASSEMBLY, GMBH/CEE	28480	8120-1689	REF
	8120-1860	*POWER CORD ASSEMBLY, CEE/CEE	28480	8120-1860	REF
	8120-2104	*POWER CORD ASSEMBLY, SEV/CEE	28480	8120-2104	REF
	8120-2956	*POWER CORD ASSEMBLY, MDPP/CEE	28480	8120-2956	REF
	8120-4211	*POWER CORD ASSEMBLY, SABS/CEE	28480	8120-4211	REF
45	8120-3445	*HP-IB CABLE ASSEMBLY, 1m, (Model 10833A)	28480	8120-3445	1

Table 6-1. Disc Drive Replaceable Parts, (Continued)

DESCRIPTION	MFR CODE	MFR PART NO.	UNITS PER ASSY
**SHAFT, switch	28480	09133-40202	1
**SHIELD, power supply	28480	09144-45404	1
*DISC DRIVE ASSEMBLY, 7941 (A1/FRA1)	28480	07941-60021	1
*DISC DRIVE ASSEMBLY, 7945 (A1/FRA1)	28480	07945-60021	REF
(Attaching Parts)			
*SCREW, machine, pnh, T15, M4.0 by 0.70, 8 mm long, w/scw	00000	OBD	3
*SCREW, machine, pnh, T10, M3.0 by 0.50, 8 mm long, w/scw	00000	OBD	1
- - - X - - -			
*CLAMP, cable	02768	8511-28-00-9901	2
*MAINFRAME ASSEMBLY	28480	07941-60074	1
**CONTACT, finger	28480	8160-0280	1
**FOOT, front	28480	09121-48303	2
**FOOT, rear	94959	SJ-5008	2
**GUIDE, PCA, 5 in. long	28480	0403-0268	2
**GUIDE, PCA, 8 in. long	28480	0403-0302	2
**GUIDE, PCA, 9.9 in. long	28480	0403-0379	2
*POWER CORD ASSEMBLY, NEMA5A/CEE	28480	8120-1378	1
*POWER CORD ASSEMBLY, BS 1363/CEE	28480	8120-1351	REF
*POWER CORD ASSEMBLY, ASC 112/CEE	28480	8120-1369	REF
*POWER CORD ASSEMBLY, GMBH/CEE	28480	8120-1689	REF
*POWER CORD ASSEMBLY, CEE/CEE	28480	8120-1860	REF
*POWER CORD ASSEMBLY, SEV/CEE	28480	8120-2104	REF
*POWER CORD ASSEMBLY, MDPP/CEE	28480	8120-2956	REF
*POWER CORD ASSEMBLY, SABS/CEE	28480	8120-4211	REF
*HP-IB CABLE ASSEMBLY, 1m, (Model 10833A)	28480	8120-3445	1



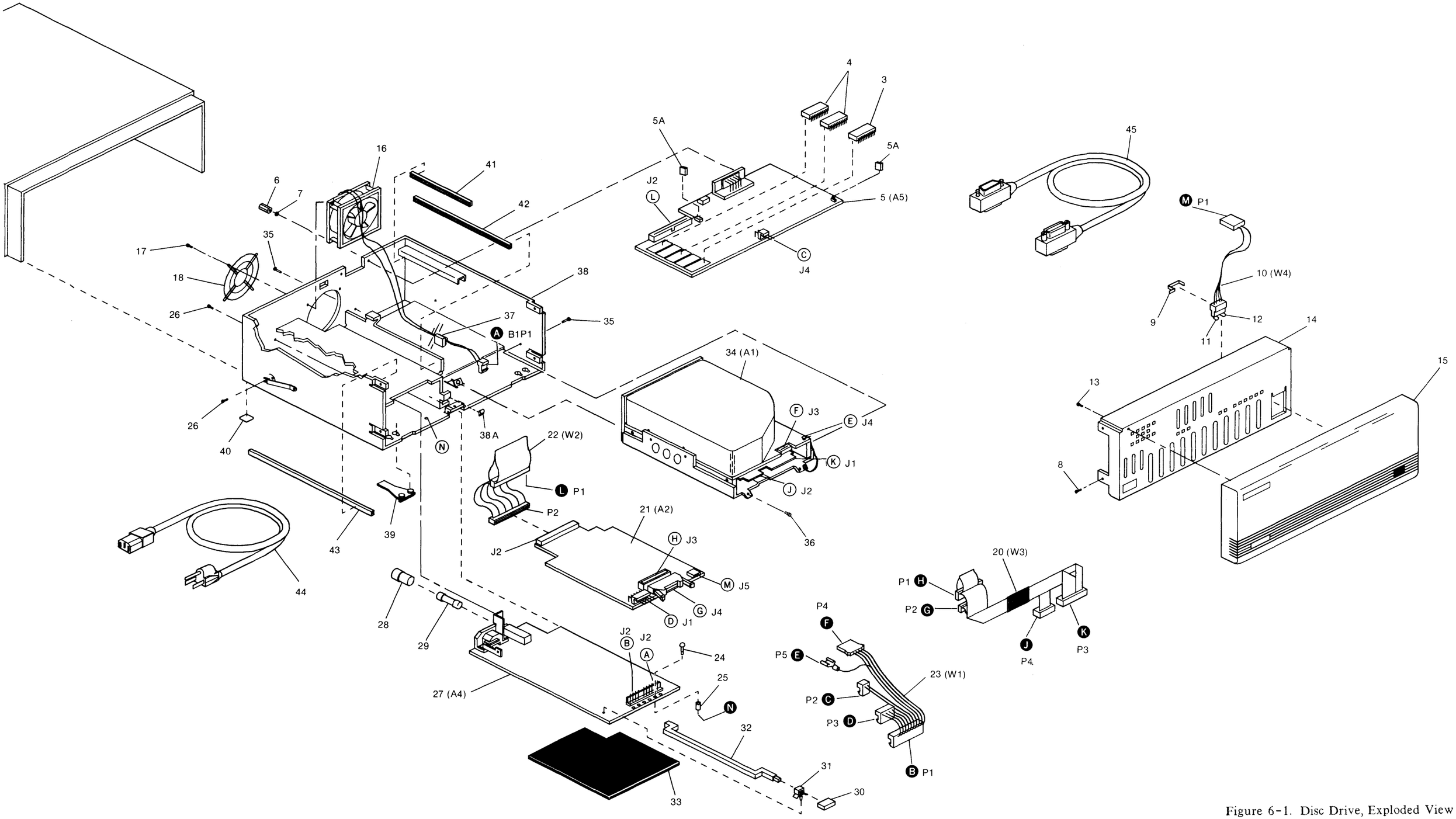


Figure 6-1. Disc Drive, Exploded View

Table 6-2. Abbreviations

A	= ampere(s)	incand	= incandescent	qty	= quantity
ac	= alternating current	incl	= include(s)	rdh	= round head
AR	= as required	intl	= internal	rect	= rectifier
assy	= assembly	I/O	= input/output	ref	= reference
		k	= kilo (10^3), kilohm	rf	= radio frequency
brkt	= bracket	kg	= kilogram	rfi	= radio frequency interference
c	= centi (10^{-2})	lb	= pound	rh	= right hand
C	= Celsius, centigrade	LED	= light-emitting diode	rpm	= revolutions per minute
cer	= ceramic	lh	= left hand	rwv	= reverse working voltage
cm	= centimetre	M	= mega (10^6), megohm	sb	= slow blow
comp	= composition	m	= milli (10^{-3})	SCR	= semiconductor-controlled rectifier
conn	= connector	mach	= machine	scw	= square cone washer
d	= deci (10^{-1})	mb	= medium blow	Se	= selenium
dc	= direct current	met oxd	= metal oxide	Si	= silicon
deg	= degree(s)	mfr	= manufacturer	slftpg	= self-tapping
dia	= diameter	misc	= miscellaneous	spdt	= single-pole, double throw
dpdt	= double-pole, double-throw	mm	= millimetre	spst	= single pole, single throw
dpst	= double-pole, single throw	mtg	= mounting	sst	= stainless steel
elctlt	= electrolytic	My	= Mylar	stl	= steel
encap	= encapsulated	n	= nano (10^{-9})	sw	= switch
ext	= external	n.c.	= normally closed	T	= TORX(R) screw
F	= Fahrenheit, farad	no.	= number	Ta	= tantalum
fb	= fast blow	NSR	= not separately replaceable	tgl	= toggle
fh	= flat head	ntd	= no time delay	thd	= thread
fig.	= figure	OBD	= order by description	Ti	= titanium
filh	= fillister head	OD	= outside diameter	tol	= tolerance
flm	= film	ovh	= oval head	U (u)	= micro (10^{-6})
fw	= full wave	oxd	= oxide	V	= volt(s)
fxd	= fixed	p	= pico (10^{-12})	var	= variable
G	= giga (10^9)	PCA	= printed-circuit assembly	Vdcw	= direct current working volts
Ge	= germanium	phh	= phillips head	W	= watt(s)
H	= Henry, Henries	pnh	= pan head	w/	= with
hd	= head	P/O	= part of	WIV	= inverse working volts
hex	= hexagon, hexagonal	pot	= potentiometer	ww	= wire-wound
hlcl	= helical	pozi	= Pozidriv		
Hz	= Hertz				
ID	= inside diameter				
in.	= inch, inches				

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Table 6-3. Code List of Manufacturers

CODE NO.	MANUFACTURER	ADDRESS
02768	Illinois Tool Works, Inc.	Des Plaines, IL
28480	Hewlett-Packard Co.	Palo Alto, CA
75915	Tracor Littlefuse Inc.	Des Plaines, IL
94959	3M Co., Adhesives, Coatings and Sealers Div.	St. Paul, MN

APPENDIX C

SECTION C

C-1. SERVICE NOTES

The following is a list of all applicable service notes for the HP 7941 and HP 7945 Disc Drives.

7941A-01
7945A-01

S E R V I C E N O T E

Supersedes: None

APPLIES TO:	All Units ☒		Only Units on Agreement ☐
PERFORM:	Immediately ☐		At PM/Normal Call ☐
	On Failure ☐		Information Only ☒
WARRANTY:	EXTENDED	NORMAL	NONE
LABOR:			X
PARTS:			X
TRAVEL:			X
SERVICE INVENTORY	Return for update ☐		Use as is ☐
	Return for salvage ☐		See text ☒
WARRANTY EXTENDED UNTIL:	N/A		

7941/45A DISC DRIVE

NEW MOUNTING TRAY AND
MAINFRAME ASSEMBLY

PARTS AFFECTED:

MOUNTING TRAY:
07941-00005 new
07941-00052 obsolete

MAINFRAME ASSY:
07941-60025 new
07941-60074 obsolete

SERIAL PREFIX INVOLVED:
2439

SYMPTOM: Replacement Disc Mechanisms (part no. 07941-69021 or 07945-69021) may not fit into 7941/45A Disc Drives with a serial prefix of 2438 or less.

CAUSE: A common mounting tray was implemented to be compatible with both 7941/45A and 7942/46A Disc Drives. The common tray is being attached to all replacement Disc Mechanisms in the pipeline for added protection during shipment and handling. Also the Mainframe Assembly needed to be redesigned to accept the new tray.

SOLUTION: If you are replacing a Disc Drive Assembly in a 7941/45A with a serial prefix of 2438 or less and this assembly has a Mounting Tray attached, then you need to remove and replace it with the tray from the defective assembly.

NOTE: The new tray and mainframe assembly are not interchangeable with either old tray or mainframe assembly. In the unlikely event that either obsoleted part needs replacement, then both the new tray and mainframe assembly need to be replaced.

HW/sg

12/84-48

9320-4766 (1/83)

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S E R V I C E   N O T E

Supersedes: 7941A-02
7945A-02

APPLIES TO:	All Units X	Only Units on Agreement ☐
PERFORM:	Immediately X	At PM/Normal Call ☐
	On Failure ☐	Information Only ☐

WARRANTY:	EXTENDED	NORMAL	NONE
LABOR:	X		
PARTS:			X
TRAVEL:			X

SERVICE INVENTORY	Return for update ☐	Use as is ☐
	Return for salvage ☐	See text ■

WARRANTY EXTENDED UNTIL: March 1, 1986

7941/45A DISC DRIVE

NEW HDC PCA
RFI MODIFICATION

PARTS AFFECTED:

PA940-60195 new
07940-69195 exchange

replaces:
07940-60095 new
07940-69095 exchange

SERIAL PREFIX: 2438

SYMPTOM: RFI emissions, although meeting specifications, are too high and could potentially exceed specifications in the future.

CAUSE: Marginal RFI emissions are radiating from the HP-IB cable.

SOLUTION: Although current units are meeting RFI specifications, all Field Stocking Inventory (FSI) of the exchange HDC Assembly part # 07940-69095) needs to be updated in the field. To update these PCA's, follow this procedure:

1.) USE ANTI-STATIC MATS AND WRIST STRAPS TO PREVENT ESD DAMAGE.

2.) SOLDER A 22 GAUGE WIRE TO JOIN PINS 12, 24, 23, AND 22 OF THE HPIB CONNECTOR ON THE CIRCUIT SIDE OF THE HDC PCA. SEE DIAGRAM ON NEXT PAGE.

3.) OBTAIN A NEW PART NUMBER STICKER (07940-69195) FROM YOUR AREA LOGISTICS MANAGER. PLACE THE NEW STICKER OVER THE EXISTING PART NUMBER ON THE PCA. DMD SERVICE ENGINEERING WILL MAIL THESE STICKERS TO THE ALM'S.

* *
* 4.) BILL DMD 1/2 HOUR LABOR. USE SERVICE CODE 20019 IN THE SERVICE *
*   CODE BLOCK ON THE CSO. *
* *

HW/sg 3/85-48

9320-4766 (1/83)

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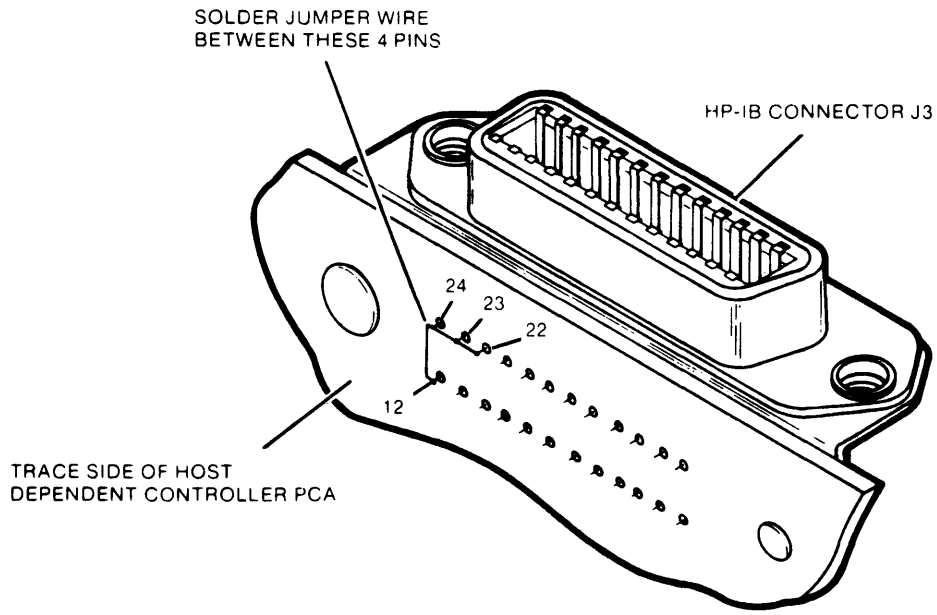
NOTE: UPDATE ALL FSI AS SOON AS POSSIBLE.

NOTE: All 7941/45A Drives with a serial prefix of 2438 or later are being shipped with the 07940-60195 PCA. Do not replace a 07940-60195 PCA or 07940-69195 PCA with a 07940-69095 PCA.

NOTE: The HDC PCA (07940-60195 or 07940-69195) is supported in both the 9144A Tape Drive and 794X Disc Drive.

NOTE: Additional stickers can be obtained from Service Engineering at DMD in Boise, Idaho or CPB at Bristol, England.



7941A-03
7945A-03

S E R V I C E N O T E

Supersedes: None

7941/45A DISC DRIVE

NEW DDC PCA

PARTS AFFECTED:

07941-60102 new
07941-69102 exchange

replaces:
07941-60002 new
07941-69102 exchange

SERIAL PREFIX INVOLVED:
2442 and greater

APPLIES TO:	All Units ☒	Only Units on Agreement ☐
PERFORM:	Immediately ☐	At PM/Normal Call ☐
	On Failure ☐	Information Only ☒

WARRANTY:	**EXTENDED**	**NORMAL**	**NONE**
LABOR:			X
PARTS:			X
TRAVEL:			X

SERVICE	Return for update ☐	Use as is ☒
INVENTORY	Return for salvage ☐	See text ☐

WARRANTY EXTENDED UNTIL: N/A

SYMPTOM: A new DDC PCA, part number 07941-60102 will be shipped with all 7941/45A Disc Drives with a serial prefix of 2442 or greater. The old DDC PCA (either 07941-60002 or 07941-69002) is functionally equivalent.

CAUSE: With the introduction of the 7942/46A Disc Tape Drives, a common DDC PCA is being introduced. The new DDC PCA, part numbers 07941-60102 or 07941-69102 have a low pass filter on the Write Fault line for greater ESD protection to the 7942/46A products.

SOLUTION: Use the 07941-69002 until gone to support 7941/45A products. The exchange DDC PCA 07941-69102 will support either the 7941/45 or the 7942/46A products.

HW/sg

1/85-48

9320-4766 (1/83)

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SERVICE NOTE

Supersedes: SUPERSEDES:

APPLIES TO:	All Units ☐		Only Units on Agreement ☒
PERFORM:	Immediately ☐		At PM/Normal Call ☒
	On Failure ☐		Information Only ☐
WARRANTY:	EXTENDED	NORMAL	NONE
LABOR:	0.5		
PARTS:	no		
TRAVEL:	no		
SERVICE INVENTORY	Return for update ☐		Use as is ☐
	Return for salvage ☐		See text ☒
WARRANTY EXTENDED UNTIL:	February 1986		

7941/45A DISC DRIVE

SHUNT BLOCK MODIFICATION

PARTS AFFECTED:

DISC MECHANISM
07941-60021 new
07941-69021 exchange
and
DISC MECHANISM
07945-60021 new
07945-69021 exchange

DRIVE SERIAL PREFIX:
2440 or less

SYMPTOM: Possible drive not ready, after replacing a DDC PCA (part nos. 07941-69002 or 07941-69102).

CAUSE: The shunt block J6 on the Disc Mechanism (part nos. 07941-60021, 07941-69021, 07945-60021, or 07945-69021).

SOLUTION: Perform the following upgrade to the Disc Mechanism on ANY failure of a drive with a serial prefix of 2440 or less:

1.) Remove the Disc Mechanism, part number 07941-6X021 or 07945-6X021 per procedure 5-11 in 7941/45A Service Manual.

2.) Remove the mounting tray attached to the bottom of the Disc Mechanism and lay the Disc Mechanism on its top to expose the component side of the Data PCA.

3.) Locate the Shunt Block J6. It is a socketted jumper block located between edge connectors J1 and J2 on the Disc Mechanism.

4.) Cut the following three shunts on the Shunt Block with an exacto knife: 7-10, 6-11, and 5-12. Only shunts 3-14, 4-13 and 8-9 should be intact on a 7941A and shunts 4-13 and 8-9 should be intact on a 7945A Disc Mechanism. Refer to the following diagram of a modified Shunt Block:

HW/rl

9320-4766 (1/83)

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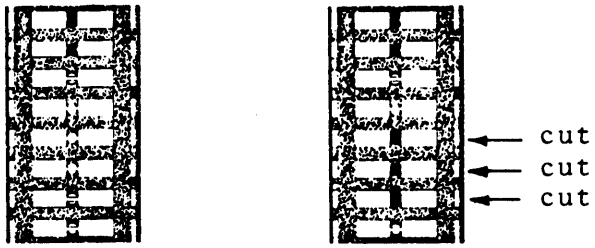
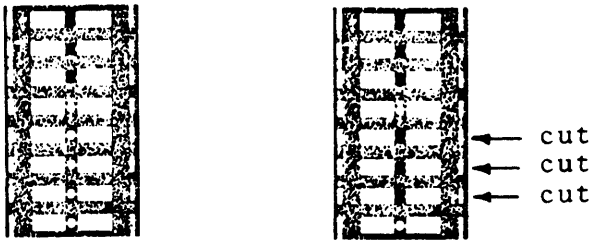
7941



7945



5.) Bill DMD 1/2 hour labor extended warranty using Serivce Code 20024 in the Service Code Block on a CSO.

NOTE: Please upgrade all Disc Mechanism's in FSI.

SERVICE NOTE

Supersedes: SUPERSEDES:

APPLIES TO:	All Units ☐		Only Units on Agreement ☐
PERFORM:	Immediately ☐		At PM/Normal Call ☐
	On Failure ☒		Information Only ☐
WARRANTY:	**EXTENDED**	**NORMAL**	**NONE**
LABOR:	.5		
PARTS:	yes		
TRAVEL:	yes		
SERVICE INVENTORY	Return for update ☐		Use as is ☐
	Return for salvage ☐		See text ☒
WARRANTY EXTENDED UNTIL:	February 1986		

7941/45A DISC DRIVE

FAULT/ON-LINE LED'S SHORTING OUT

PARTS AFFECTED:

Cable Assembly
07941-60033
and
Grounding Strap
07941-60011

DRIVE SERIAL PREFIX:
2501 or less

SYMPTOM: The red and green LED's on the front of the disc drive short out, causing the LED's to go off.

CAUSE: The ground strap (part no. 07941-60011) which grounds the Disc Mechanism (part nos. 07941-60021, 07941-69021, 07945-60021, or 07945-69021) to the mainframe assembly presses against the On-line and Fault LED's (part no. 07941-60033).

SOLUTION: On failure, place 1 3/4 inches of shrink tubing (part no. 08900312, .25 ID shrink tubing) over the grounding strap.

Bill DMD warranty for labor, travel, and materials using Service Code number 20025 in the Service Code Block on a CSO.

HW/rl

9320-4766 (1/83)

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7941A-06
7945A-06

S E R V I C E N O T E

Supersedes:

APPLIES TO:	All Units ☒	Only Units on Agreement ☐
PERFORM:	Immediately ☐	At PM/Normal Call ☒
	On Failure ☐	Information Only ☐

WARRANTY:	EXTENDED	NORMAL	NONE
LABOR:	0.5 hr		
PARTS:	yes		
TRAVEL:	no		

SERVICE	Return for update ☐	Use as is ☐
INVENTORY	Return for salvage ☐	See text ☒

WARRANTY EXTENDED UNTIL: June 1986

7941/45A DISC DRIVE

NEW FIRMWARE-EXEC AND
DISC CODE

PARTS AFFECTED:
07940-10105 Exec Eprom kit
07940-10203 Disc Eprom kit

REPLACES:
07940-10104 Exec Eprom kit
07940-10202 Disc Eprom kit

DRIVE SERIAL PREFIX:
2503 or less

SYMPTOM: The disc drive does not properly recover from an off track condition during a seek. This causes faults to be logged when there is no actual defect in the mechanism. Commonly entered faults codes are 135 (87 hex), 171 (AB hex) and 53 (35 hex).

CAUSE: The previous revisions of Disc Code would initiate a seek before checking for an offtrack condition. If there was an offtrack condition, the seek would fail with a Seek Fault indication.

SOLUTION: The new Disc Code (EPROM Kit no. 07940-10203) checks for any offtrack condition before issuing a seek. If a seek fails the first time, the firmware allows for one seek retry before issuing a Seek Fault.

On next service call, update the firmware to the new version. Disc drives with a serial prefix of 2442 or less require a new version of both the Disc Code (EPROM Kit no 07940-10203) and Exec Code (EPROM Kit no. 07940-10105). Disc drives with a serial prefix between 2443 and 2503 inclusive, require only the Disc Code.

Install the new firmware according to the following socket locations on the HDC PCA (part nos. 07940-60095, 07940-69095, 07940-60195, or 07940-69195).

HW/rl

9320-4766 (1/83)

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EPROM KIT	SOCKET	PART NUMBER	
07940-10203	U131	07940-89031	Disc Code
	U161	07940-89032	Disc Code
07940-10105	U101	07940-89050	Exec Code

The individual EPROMS are not orderable.

Bill DMD warranty for labor and parts only using Service Code number 20028 in the Service Code Block on a CSO for any disc drive with serial prefix 2503A or less.

Bill CPB warranty for labor and parts only using Service Code number 20028 in the Service Code Block on a CSO for any disc drive with serial prefix 2503E or less.

Disc Drives with a serial prefix of greater than 2503 have an acceptable revision of firmware. Acceptable part numbers for the individual EPROMS are given below. Any lower number is unacceptable.

DISC CODE	EXEC CODE
07940-89031	07940-89030
07940-89032	07940-89040

NOTE: All FSI should be rolled to the new firmware. The new Eprom Kits 07940-10203 and 07940-10105 are available from CPC. The old Eprom kits (part nos. 07940-10101, 07940-10102, 07940-10103, 07940-10104, 07940-10201, and 07940-10202) are obsolete and should be returned for credit to CPC.

NOTE: Exec Eproms 07940-10103, 07940-10104 and 07940-10105 have identical operation in 7941/45A Disc Drives. FSI is being rolled to 07940-10105 to maintain compatibility with all 7942/46A Disc/Tape Drives.

NOTE: The following Fault Codes have been added with the 07940-10203 revision of Disc Code.

Oct	Dec	Hex	Unit Faults (P8 contains Disc Controller IC Error Register)
160	112	70	Write Fault on retry of seek
161	113	71	Drive not ready on retry of seek
162	114	72	Seek retry fault
163	115	73	Scan ID failed before retry of seek
164	116	74	Seek timeout fault - 3 secs.
165	117	75	Seek retried
166	118	76	Seek retry timed out - 300 msecs.

7941A-07
7945A-07

SERVICE NOTE

Supersedes: None

7941/45A Disc Drive

DDC PCA - Rev 2427
Address Mark Errors

Parts Affected:
07941-60002 new
07941-69002 exchange

Drive Serial Prefix:
2434 or less

APPLIES TO:	All Units ☒		Only Units on Agreement ☐
PERFORM:	Immediately ☐		At PM/Normal Call ☐
	On Failure ☒		Information Only ☐
WARRANTY:	**EXTENDED**	**NORMAL**	**NONE**
LABOR:	0.5		
PARTS:	yes		
TRAVEL:	no		
SERVICE	Return for update ☒		Use as is ☐
INVENTORY	Return for salvage ☐		See text ☐
WARRANTY EXTENDED UNTIL:	June 1986		

Symptom: When a Disc Mechanism (part no's. 07941-60021 new, 07941-69021 exchange, 07945-60021 new, and 07945-69021 exchange) is changed, the replacement Disc Mechanism may exhibit a high error rate. The errors typically occur as address mark errors on all heads. They are reported with the External Exerciser as error byte 10000010. This type of error is fully recoverable and will only be seen when error rate testing is performed and not during run time.

Cause: There was an instability in the phase lock loop circuitry on the DDC PCA's (part no's. 07941-60002 new, and 07941-69002 exchange) with date code of 2727 or less. This slight instability is usually of no concern, but may cause a problem with a small percentage of disc mechanisms. Thus when a Disc Mechanism is changed, the new Disc Mechanism may not operate properly with the old DDC.

Solution: The DDC PCA was redesigned to provide a more stable phase lock loop which will function properly with all disc mechanisms. This improvement is included in all DDC PCA's with a revision number of 2428 or greater and is also included on the new version DDC PCA (part no. 07941-60102 new, 07941-69102 exchange).

Since error rate testing is time consuming, we recommend that an updated DDC PCA be installed whenever the disc mechanism is replaced if the old DDC PCA has a revision of 2427 or less.

HW/rl 5/85-48

9320-4766 (1/83)

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Bill DMD warranty for labor and the DDC PCA. Use Service Code number 20029 in the Service Code Block on a CSO.

NOTE: Retrun for credit any DDC PCA (part no. 07941-69002) with a revision number of 2427 or less in Field Stocking Inventory (FSI).

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